F-77A

PDP-7 MAINTENANCE MANUAL

DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS

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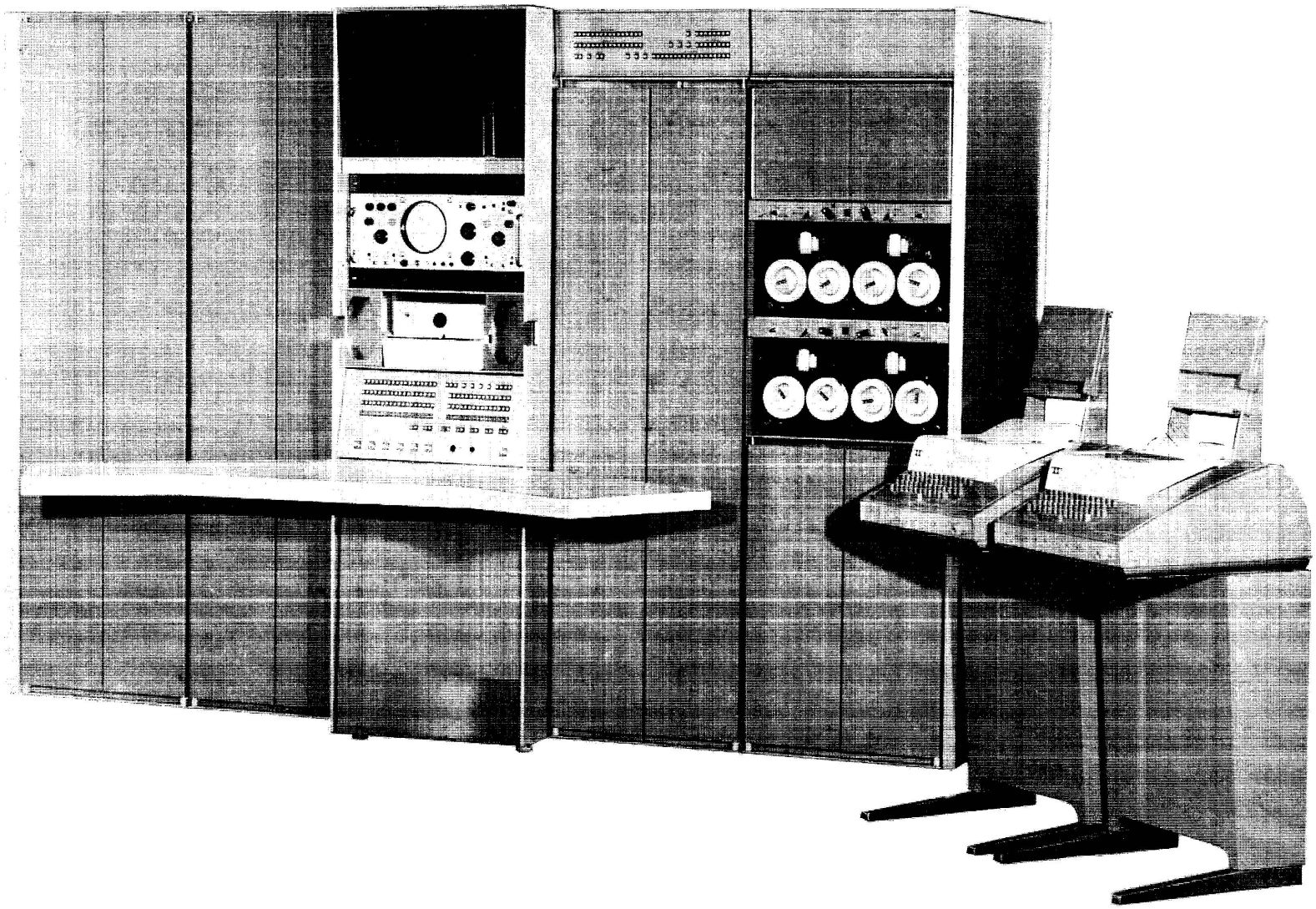

Figure 1-1 Programmed Data Processor-7

CHAPTER 1
INTRODUCTION AND DESCRIPTION

1.1 INTRODUCTION

The Programmed Data Processor (PDP-7), manufactured by Digital Equipment Corporation, is a general purpose stored program computer using solid state FLIP CHIP™ logic modules. The machine is a single address type, with fixed 18-bit word length, and uses 1s complement and 2s complement notation to facilitate multiprecision arithmetic.

The manual describes the basic computer organization and its optional equipment, and includes logic discussions in terms of the machine instruction repertoire. Manual operations and sample diagnostic programming routines also are included for maintenance purposes. This manual is applicable to PDP-7 machines having serial numbers 100 and above.

1.2 PURPOSE

This manual is compiled with a dual purpose--to provide initial instruction in the PDP-7 system, and to provide maintenance information in a form for easy use and quick reference.

Information in this manual is graded for use by engineers and technicians familiar with digital logic techniques, digital computer principles, and the concepts of computer programming. Programmed maintenance routines greatly facilitates maintenance of this equipment.

One of several documuments related to the PDP-7 computer, this manual provides an understanding of system organization and capabilities. Each chapter is oriented to contain sufficient information for maintaining the equipment. The levels of discussion in any case assume the user to be familiar with the technology of similar computers. For complete and comprehensive coverage of areas not found in this manual, the operator should refer to the list of documents in paragraph 1.7.

1.3 SCOPE

In addition to information necessary for proper operation and maintenance, this manual describes in detail input/output and standard optional equipment used with the PDP-7 and core memory.

The presentation is both hardware and program oriented, and contains sufficient descriptions and detailed logic drawings for understanding the logical operations of the system. At the same time, descriptions and treatment are program oriented so that the software operations and implications, particularly for

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maintenance, are thoroughly understandable. Most important, the book is formatted and organized in such a manner that any reference can be easily located.

1.4 PHYSICAL DESCRIPTION

The basic PDP-7 is completely self-contained in a 3-bay DEC metal cabinet, and requires no special power sources, air conditioning, or floor bracing. A door (held closed by a magnetic latch) at the front provides access to the wiring side of all module mounting panels. A fan at the cabinet bottom draws air through a dust filter to cool the modules. Air passes over the modules and exits through louvers at the top.

1.4.1 Equipment Supplied

Figure 1-2 shows the component locations of the basic PDP-7. The paper tape punch and reader are mounted on the front panel. The Teletype unit may be mounted on a separate stand or may be placed on the console table. For additional physical data, see paragraph 1.8, System Specifications.

1.5 OVERALL SYSTEM CONFIGURATION

The standard PDP-7 system includes the processor, memory, and the standard input/output equipment shown in the processor block of figure 1-3. All other elements shown are optional equipment.

The processor performs the logical and arithmetic functions, controls the storage and retrieval of information in core memory and controls flow of information to and from peripheral equipment. The processor consists of control logic and the major registers of the system. The operator console associated with the processor permits manual manipulation of the contents of memory.

The core memory is a 4096-word or 8192-word random access ferrite core memory. The basic memory is expandable to a maximum capacity of 32,768 words by using added memory modules and a Memory Extension Control Type 148. The memory has a cycle time of 1.75 μsec and provides a computation rate of 285,000 additions per sec. Indirect addressing and autoindexing features provide programming flexibility.

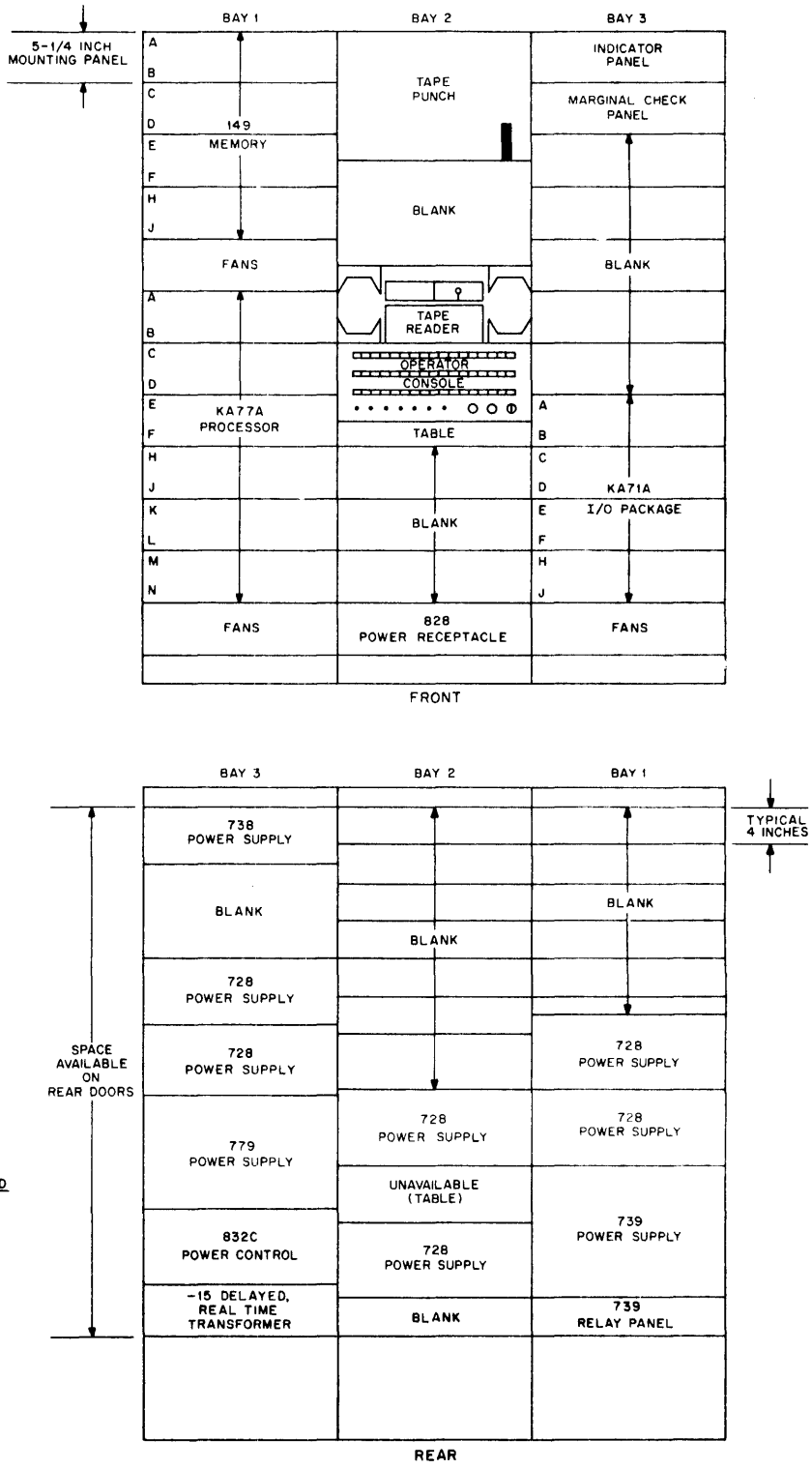
The standard input/output (I/O) configuration contains the following peripheral equipment:

Teletype KSR Unit

Paper Tape Reader and Control

The Teletype keyboard inserts data into the computer, and the Teletype unit types out data on page size roll paper, under either manual or program control.

The paper tape reader reads data from punched paper tape photoelectrically, controlled by the computer stored program. The paper tape punch provides output on punched paper tape, controlled by the stored program.



REAR SPACE REQUIREMENTS

EQUIPMENT TYPE	VERTICLE SPACE REQ'D
728A POWER SUPPLY	8 INCHES
734A,B,C POWER SUPPLY	8 INCHES
743A POWER SUPPLY	12 INCHES
772A POWER SUPPLY	8 INCHES
778A POWER SUPPLY	12 INCHES
779A POWER SUPPLY	12 INCHES
832 POWER CONTROL	8 INCHES

Figure 1-2 PDP-7 Component Locations

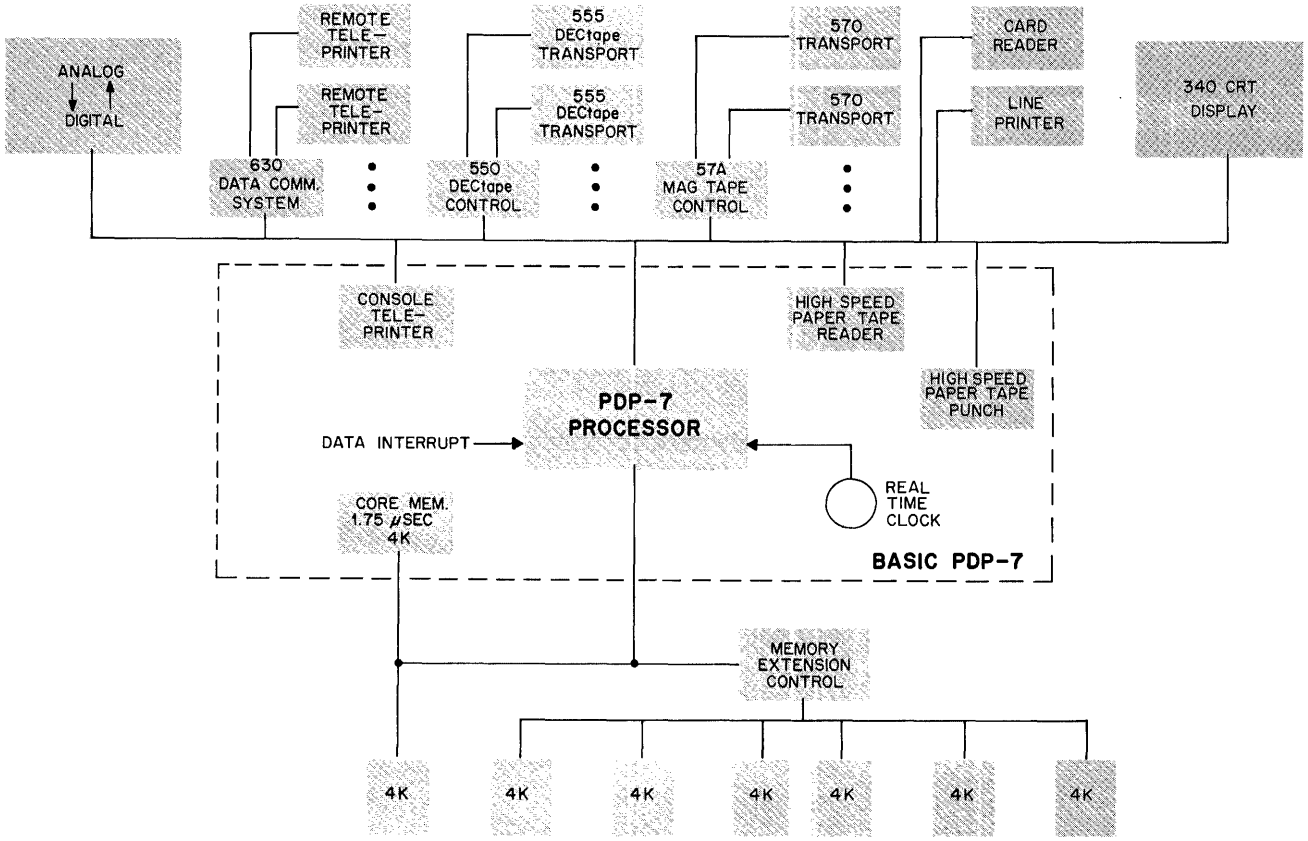


Figure 1-3 PDP-7 System Diagram

The interface basically provides control links between the processor and input/output peripheral equipment. In this instance, input and output data passes through the interface unit, which interleaves high-speed data transfers and priority selection of input and output devices seeking communication with the computer.

1.6 OPTIONS

The design of the PDP-7 offers flexibility for increasing the capacity and precision of the system by selection of a wide variety of optional peripheral equipment. Location requirements depend on the nature of the option and on availability of space (see User Handbook, F-75A, for typical installation and layout configurations).

1.6.1 Standard Options

For practical purposes, options are classified as either standard or special in accordance with projected requirements of the customer. A typical PDP-7 installation using many of the standard options

available is shown on figure 1-4. These options, described fully in chapter 4, are of three types: input and output options, processor options (not shown), and memory expansion options. A wide variety of input/output options are offered for use with the PDP-7, and these units are listed and device characteristics described in table 1-5. The standard processor options are Extended Arithmetic Element Type 177 (EAE), Automatic Priority Interrupt Type 172 (API), Data Interrupt Multiplexer Type 173, Memory Increment Type 197, and Boundary Register and Control Type KA70A.

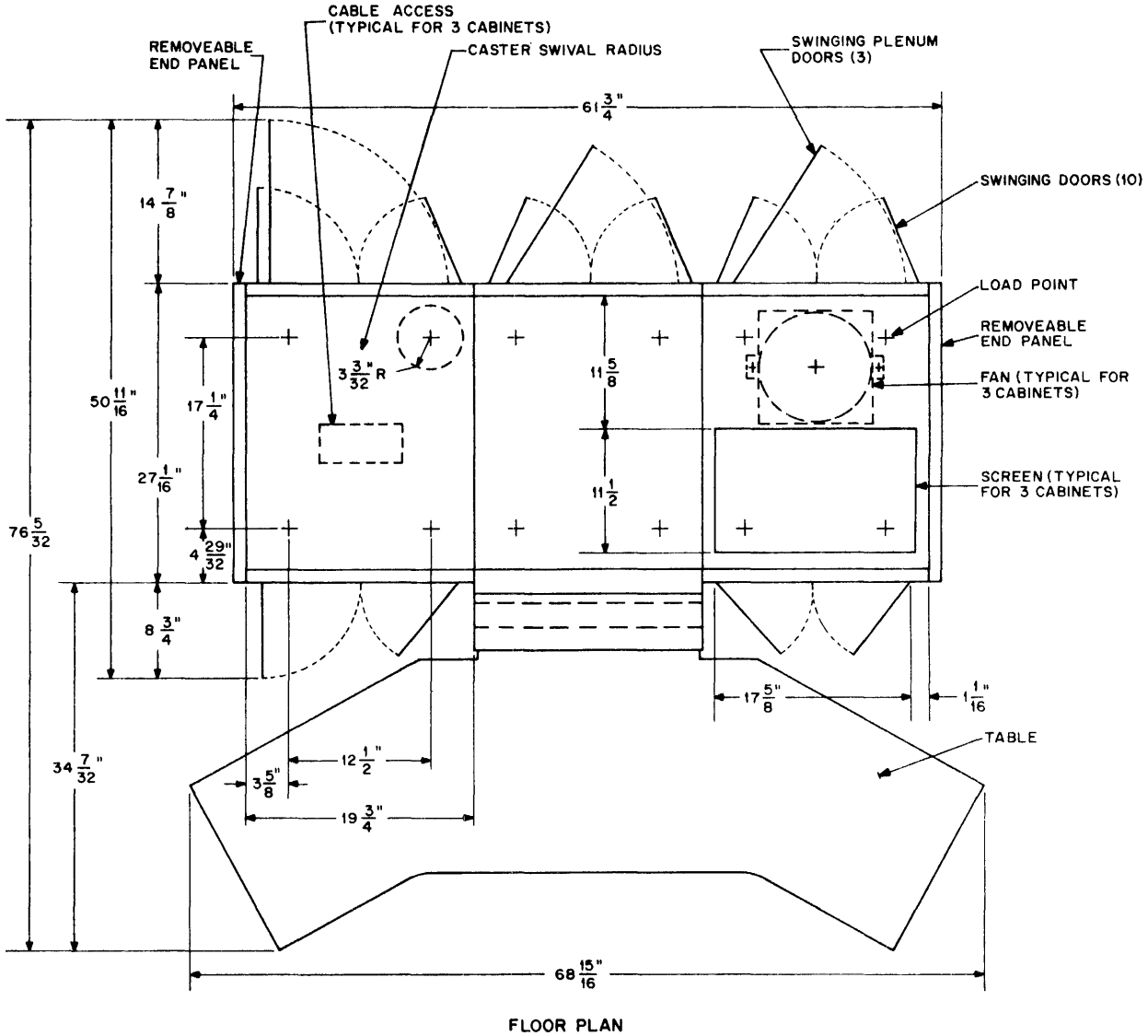


Figure 1-4 Typical PDP-7 Installation

The EAE option facilitates high-speed multiplication, division, shifting, normalizing, and register manipulation. Installation of the EAE adds an 18-bit multiplier quotient register (MQ) to the

computer as well as a 6-bit step counter register (SC), and the content of the MQ is continuously displayed on the operator console. The Type 177 option and the basic computer cycle operate asynchronously, permitting performance of computations in the minimum possible time. Further, the EAE instructions are microcoded so that several operations can be performed by one instruction to simplify arithmetic programming. Average multiplication time is 6.1 μsec; average division time is 9 μsec.

The Automatic Priority Interrupt Type 172 increases the capacity of the PDP-7 to handle transfers of information to and from input/output devices by directly identifying an interrupting device, without flag searching. Multilevel program interrupts are permissible where a device of higher priority supersedes an interrupt already in process. These functions increase the speed of the input/output system and simplify the programming, thereby servicing efficiently more and faster devices. The Type 172 contains 16 automatic interrupt channels arranged in a priority sequence so that channel 0 has the highest priority and channel 17_8 has the lowest priority. The priority chain guarantees that if two or more I/O devices request an interrupt concurrently, the system grants the interrupt to the device with the highest priority. The other interrupts will be serviced afterwards in priority order.

Using the Data Interrupt Multiplexer Type 173, the single PDP-7 data break interrupt channel is expanded to handle information transfers with three high-speed I/O devices. This option provides multiplex control for simultaneous operation of three high-speed devices such as magnetic tapes or drums. Maximum combined transfer rate is 570,000 18-bit words/sec.

The Memory Increment Type 197 option allows an external condition or signal from an I/O device to increment the contents of any core memory location. The peripheral device initiates a break cycle so that the contents of a core memory address specified by the device are read into the memory buffer register, incremented by one, and written back into the same address in one computer cycle.

The Boundary Register and Control Type KA70A option establishes core memory address boundaries that can be assigned to specific users when the system is used for real-time computing with simultaneous multiuser program execution.

The standard core memory options are Memory Extension Control Type 148, Expansion Modules Type 147 and 149B, and Memory Parity Type 176.

Memory Extension Control Type 148 is used when expanding memory capacity beyond 8K words. This option provides the necessary extension of the program counter, memory address register, and mode control.

Any memory size from 4096 to 32,768 words can be obtained by addition of Core Memory Modules Type 147 or 149B. Type 147 extends the capacity of the standard 4096 word memory to 8192 words. Type 149B extends memory capacity by one field of 8192 words. Type 149B can be added only to memories of 8K, 16K, or 24K capacity (not to 4K, 12K, etc., without also adding a Type 147 module).

Memory Parity Type 176 option assures reliability of all core memory data storage and retrieval operations by generating, storing, and checking parity on every transfer. An odd parity bit is generated and written in the same core location as the word being written. Upon reading, a word drawn from core memory is checked for parity, and, if odd parity is detected, a program interrupt is initiated or the program is halted.

1.6.2 Special Options

Special options available with the PDP-7 system are not discussed in detail in this manual. Information is provided on a customer-need basis and reference is supplied to the proper available vendor documents covering peripheral equipment supplied but not manufactured by Digital Equipment Corporation.

Most special options are input/output devices. Often the interface logic for each device varies in accordance with the data transfer speed of the device and to its relative importance to the program. Slow-, medium-, and high-speed devices are connected as program controlled transfer channels, data channels, and direct memory access channels. Medium- and high-speed devices are often connected as automatic priority interrupt channels. Chapter 3 contains discussions of these interface control channels, and chapter 4 contains a list of available special options they control.

1.7 REFERENCE DOCUMENTS

Tables 1-1 and 1-2 list the standard documentation provided for the PDP-7 system. Other documents may be furnished as applicable to customer requirements.

TABLE 1-1 HARDWARE AND SOFTWARE DOCUMENTATION

Document	Description
FLIP CHIP Module Catalog, C-105	Function and specifications of FLIP CHIP modules and accessories
System Module Catalog, C-100	Function and specifications of system modules and accessories
PDP-7 User Handbook, F-75A	Programming, instruction format, and computer functions
PDP-7 Software Package	Perforated program tapes and descriptions for symbolic assembly language, utility subroutines and Maindec (maintenance) programs (see table 1-2)

TABLE 1-1 HARDWARE AND SOFTWARE DOCUMENTATION (continued)

Document	Description
Instruction manuals and maindec programs for I/O devices	Individual manuals and programming material available on a customer-need basis
Tech. Manual, KSR-33, vols 1 and 2 Bulletin 273B	Operation and maintenance instructions
Parts, Model 33 Page Printer Set, Bulletin 1184B	IPB for Teletype unit
Tech. Manual, Hi-Speed Tape Punch Set Bulletin 215B (BRPE)	Operation and maintenance instructions
Manual Model 2500 Perforated Tape Reader	Operation and maintenance instructions

TABLE 1-2 MAINTENANCE PROGRAM LIBRARY

Name	Number
Maindec 702 (Address Test)	Digital-7-55-M
Maindec 703 (Checkerboard)	Digital-7-56-M
Maindec 701 (Instruction)	Digital-7-54-M
Contest II (Instruction)	Digital-7-52-M
Teleprinter Test	Digital-7-50-M
Maindec 710 (Reader)	Digital-7-57-M
Reader Punch Test	Digital-7-53-M
Clock Interrupt	Digital-7-51-M
Options	
Automatic Priority Interrupt Test	Digital-7-59-M
Extended Arithmetic Element Test	Digital-7-58-M
DECTOG	Digital-7-20-10
57A Error Specification	Digital-4-57-M

TABLE 1-2 MAINTENANCE PROGRAM LIBRARY (continued)

Name	Number
Options (continued)	
340 Display Diagnostic	Digital-7-63-M
34 Display Test	Digital-7-60-N
370 Light Pen Test	Digital-4-3-I
Drum Diagnostic	Digital-7-62-M
630 Diagnostic	Digital-7-64-M

1.8 SYSTEM SPECIFICATIONS

The following tables, 1-3, 1-4, and 1-5, summarize the properties of the PDP-7 system and some of the available standard options.

TABLE 1-3 PHYSICAL DIMENSIONS

Unit	Ht. (in.)	Width (in.)	Depth (in.)	Wgt. (lbs)
Cabinet	69-1/8	61-3/4	33-9/32	1130
Table		68-15/16	19-7/8	
Teletype	8-3/8	18-5/8	18-1/2	40

TABLE 1-4 SUMMARY OF SYSTEM PERFORMANCE CHARACTERISTICS

Function	Capability
Computer type	Parallel binary, single address, fixed 18-bit word length
Machine code	1s and 2s complement notation
Memory	Coincident current ferrite core
Standard capacity	4096 or 8192 words
Optional capacity	Expandable to 32,768 words
Cycle time	1.75 μsec

TABLE 1-4 SUMMARY OF SYSTEM PERFORMANCE CHARACTERISTICS (continued)

Function	Capability
Computation rate	285,000 additions/sec
Transfer rate	
Data interrupt	570,000 words/sec
Addressing	Single address with indirect addressing
Instructions	16 basic (13 memory reference, 3 augmented). Augmented instructions are microprogrammed to provide more than 175 commands.
I/O capability	Standard, 64 different devices individually selected and addressed
Standard I/O lines	
Device selector	expandable to any number
Information collector	seven 18-bit channels
Information distributor	six 18-bit channels
Signals	
Levels	0v and −3v
Pulses	
Power requirement	Standard, single source, 115v, 60 cps, single phase Optional, 220v, 50 or 60 cps
Power dissipation	2200 watts
Heat dissipation	7150 Btu per hour
Ambient conditions	
Operating temperature	50 to 122°F
Operating humidity	0 to 90% relative humidity
Storage temperature	32 to 122°F
Storage humidity	less than 90%

TABLE 1-5 SUMMARY OF PERIPHERAL EQUIPMENT CHARACTERISTICS

Unit	Capability
Basic PDP-7 I/O Equipment	
Type KSR-33 Teletype	10 char/sec ACSII standard 8-bit code
Type 2500 Paper Tape Reader	300 char/sec
Type BRPE Paper Tape Punch	63.3 char/sec
Standard I/O Options	
Type CR01B Card Reader and Control	100 cards/min, 12 row, 80 col cards; alpha-numeric or binary
Type 421 Card Reader and Control	200 cards/min, (800 Type 421B); alpha-numeric or binary
Type 40 Card Punch and Control	Controls card punch 1 row at a time at 40 msec intervals (100 cards/min)
Type 647 Automatic Line Printer and Control	Selection, 64 characters; line length 120 characters; print rate, 300, 600 or 1000 lines/min. Loading, printing and format under program control.
Type TU55 DECtape and Control Type 550	Fixed address, magnetic tape; read, write, and search speed, 80 ips; recording density, 375 bpi; storage, 3 million bits; prerecorded timing and mark tracks
Type 57A Automatic Magnetic Tape Control	Controls up to 8 IBM or IBM compatible tape transports. Controls to read or write at densities of 200, 556 or 800 char/in.; speed, 75 or 112.5 ips.
Type 570 Magnetic Tape Transport	Reads and writes at 75 or 112.5 ips at program selected densities of 200, 556, or 800 char/in. IBM compatible.
Type 545 Magnetic Tape Transport	Speed, 45 ips; densities of 200, 556 or 800 bpi. IBM compatible.

TABLE 1-5 SUMMARY OF PERIPHERAL EQUIPMENT CHARACTERISTICS (continued)

Unit	Capability
Standard I/O Options (continued)	
Type 50 Magnetic Tape Transport	Use with Type 57A to read/write IBM compatible tapes; transfer rates of 15,000 or 41,700 char/sec; tape speed, 75 ips at densities of 200 or 556 char/in.
Type 24 Serial Drum System	Block transfers through data interrupt facility by interlaced program and drum transfer operation. Storage, 32,768; 65,536; or 131,072 words.
Type 350 Incremental Plotter Control	Controls 1 Digital Incremental Recorder, made by California Computer Products, for high-speed point plotting, continuous curves, etc.
Type 34A Oscilloscope Display	Displays data point-by-point on 5-inch scope. Horizontal axis to 10 binary bits; vertical axis to 10 binary bits.
Type 30D Precision CRT Display	Random positioning point plotting; 16-inch CRT; raster, 9-3/8 in. square with 1024 points per side. Plotting rate is 35 μsec per point.
Type 340 Precision Incremental CRT Display	
Raster	9-3/8 in. square
Plotting rate	1.5 μsec per point in vector, increment, and character modes
Random point plotting rate	35 μsec
Types 33 and 342 Symbol Generators	Type 33 used with Type 30D Display Type 342 used with Type 340 Display
Type 370 Photomultiplier Light Pen	High-speed detection of display on Types 34A, 30D and 340 Displays. Computer samples detection to alter program.

TABLE 1-5 SUMMARY OF PERIPHERAL EQUIPMENT CHARACTERISTICS (continued)

Unit	Capability
	Standard I/O Options (continued)
Type 138E Analog-to-Digital Converter	Successive approximation type; input range, 0 to 10v; converted binary, selectable from 6 to 12 bits. Combinations of switching point accuracy and number of bits are switch selectable.
Type 142 Analog-to-Digital Converter	High-speed converter; converts to a single 10-bit binary number in 6 μsec. Conversion accuracy is ± 0.15%, ± 1/2 LSB.
Type 139E Multiplexer and Control	Select up to 64 analog input channels for use with Types 142 or 138E
Types ADA-1 Analog-Digital-Analog Converter	For fast real-time conversion between digital and analog computers
Max sample rate D/A	200 kc
Max sample rate A/D and interface	100 kc
Word length	ten bits
Type 630 Data Communication System	Real-time interface with Teletype stations. Available for half-duplex and full-duplex operation with up to 64 stations.
Type 140 Relay Output Buffer	Inputs from computer accumulator to actuate 18 relays to provide either direct digital control or signal generation for external equipment
Type 195 Inter-Processor Buffer	Provides interface with another computer for bidirectional data communication asynchronously

1.9 REFERENCING CONVENTIONS

The Digital Equipment Corporation engineering drawing conventions and instruction manual referencing should be understood at this point. A study of the reference conventions in this paragraph and chapter 6 will save considerable time and preserve thought continuity when reading the text that follows. Any reference to figure numbers or table numbers indicates that the illustration or table is located in the denoted chapter. For example, figure 3-1 is located in chapter 3, and is the first illustration in that chapter.

All engineering drawings have a full drawing number. These drawings are included in chapter 6. In text, references to engineering drawings are abbreviated in the following manner:

Full Drawing No.	D-KA77A-0-2	← Drawing No. of Set
		← Processor Drawing Set No.
First text reference	KA77A-2	
All other text references	-2	

To locate a specific signal or function, the origin of the signal on a specific drawing is stated in one of two conventions.

Example 1

"The BGN pulse developed at PA(D23,4)" where

PA - Module Type
D23 - Physical Location of Module
4 - Specific drawing number of previously mentioned set.

For complex block schematics the second convention is used.

Example 2

"The CLR pulse generated at Module PA(2:C4)" where

PA - Module Type
2 - Specific drawing number of previously mentioned set
C4 - Roadmap coordinate location on drawing.

CHAPTER 2
OPERATION

2.1 INTRODUCTION

This chapter provides sufficient operating information for a technician acquainted with computer systems similar in scope to the PDP-7, and contains descriptions in tabular form of all system controls and indicators, references for detailed information, and a discussion of maintenance programming considerations for the operator. To become fully cognizant of programming maintenance procedures for the PDP-7, the operator must assimilate the information in this chapter along with the diagnostic routines in chapter 5, assuming he has previously digested the programming and operating discussions found in the PDP-7 User Handbook, F-75A.

2.2 SYSTEM CONTROLS AND INDICATORS

The following pages contain tables that list and define all system manual controls and indicator lights. These are arranged on the following system elements (see figure 1-2): operator console, indicator panel, Teletype console, and perforated tape reader unit. On all panels, an indicator light "on" denotes a binary 1 in the associated register bit or the flip-flop control function.

The operator console and the indicator panel contain all major controls and indicators for manual manipulation and for monitoring system operations. The operator console has major operating controls such as STOP, START, CONTINUE, etc., and switches for selecting processor accumulator contents and memory addresses for inserting data into the processor. During continuous operation this panel displays the major processor register contents and various status conditions. The indicator panel displays memory conditions and both status and contents of functions and registers associated with the standard input/output facility.

2.2.1 Operator Console Controls and Indicators

The operator console appears in figure 2-1, and table 2-1 lists the functions of the controls and indicators.

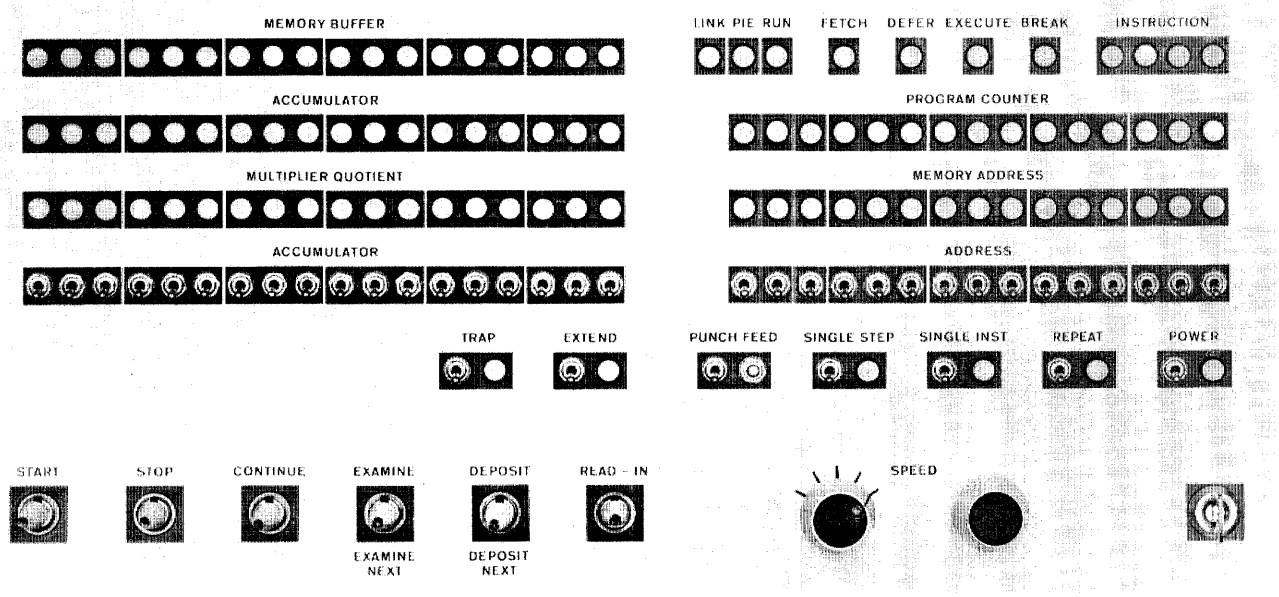


Figure 2-1 Operator Console

TABLE 2-1 OPERATOR CONSOLE CONTROLS AND INDICATORS

Control or Indicator	Function
START key	Starts the processor. The first instruction is taken from the memory cell specified by the setting of the ADDRESS switches. The START operation clears the accumulator (AC) and link (L), and turns off the program interrupt facility.
STOP key	Stops the processor at the completion of the memory cycle in progress.
CONTINUE key	Causes the computer to resume operation from the point at which it was stopped. Besides the normal off and momentary on positions, this key has a latched-on position obrained by raising the key instead of depressing.
EXAMINE key	Places the contents of the memory cell specified by the ADDRESS switches into the AC and memory buffer (MB). This operation is accomplished by automatically performing a LAC instruction (see User Handbook) when the EXAMINE key is pressed. At the completion of the operation, memory address register (MA), holds the contents of the ADDRESS switches and the program counter (PC) contains the address of the next cell.

TABLE 2-1 OPERATOR CONSOLE CONTROLS AND INDICATORS (continued)

Control or Indicator	Function
EXAMINE NEXT key	Places the contents of the cell specified by the PC into the AC and MB. The contents of the PC are incremented by 1, and the MA contains the address of the register examined.
DEPOSIT key	Deposits the contents of the ACCUMULATOR switches into the memory cell specified by the ADDRESS switches. This operation is accomplished by automatically performing tasks similar to the combination of the CLA, OAS, and DAC instructions (refer to Handbook) when the DEPOSIT key is pressed. The contents of the ACCUMULATOR switches remain in the AC and MB. The contents of the ADDRESS switches appear in the MA. The PC contains the address of the next cell.
DEPOSIT NEXT key	Deposits the contents of the ADDRESS switches into the memory cell specified by the PC. The contents of the PC are then incremented by 1. At the completion of the operation, the contents of the AC and MA are the same as for the DEPOSIT operation.
READ-IN key	Punched paper tape is read in binary mode and stored in a core memory block when this key is pressed and released. The ADDRESS switches supply the first address of the memory block. After reading the tape, program control transfers to the processor which executes the last instruction word stored in the block. To indicate that this last computer word on tape is the instruction to be executed next, a hole must be punched in channel 7 of the last line of the three binary lines that constitute the last word.
SPEED switch and control	These two controls vary the repetition rate of manual operations from approximately 40 μsec to 8 sec. The switch (left) is a 5-position coarse control; the control, (right) is a continuously variable fine control. Slowest speed is obtained with both controls in the fully counterclockwise position.

TABLE 2-1 OPERATOR CONSOLE CONTROLS AND INDICATORS (continued)

Control or Indicator	Function
Console lock	This key-operated, 2-position lock switch prevents inadvertent key operation from disturbing a program in progress. When the key is turned counterclockwise, the console is unlocked and all controls operate normally. When the key is turned clockwise, the console is locked; operation of any of the console keys, the SPEED controls, or the POWER, SINGLE STEP, SINGLE INST, or REPEAT switches does not affect the operation of the computer. The program, even with the keys disabled by the lock, can monitor the status of the ACCUMULATOR switches.
TRAP switch and indicator	Permits the program to enter the trap mode.
EXTEND switch and indicator	In the raised position, this switch allows the extend mode to be enabled by the EXAMINE and DEPOSIT keys. The indicator lights to denote enabling of the extend mode control.
PUNCH toggle switch and FEED pushbutton	The toggle switch controls application of primary power to the perforated tape punch. When the switch is down, punch power is under program control; when up, punch power is on. The pushbutton causes the perforated tape punch to punch tape leader. Punch power remains on for an additional 5 sec as it does under program control.
SINGLE STEP switch and indicator	This switch causes the computer to stop at the completion of each memory cycle. Repeated operation of the CONTINUE key while this switch is on steps the program one memory cycle at a time. The indicator lights to denote operation in the single-step mode.
SINGLE INST switch and indicator	This switch causes the computer to stop at the completion of each instruction. Repeated operation of CONTINUE key with this switch on steps the program one instruction at a time.

TABLE 2-1 OPERATOR CONSOLE CONTROLS AND INDICATORS (continued)

Control or Indicator	Function
	When both switches are on, SINGLE STEP takes precedence over SINGLE INST. The indicator lights to denote operation in the single-instruction mode.
REPEAT switch and indicator	This switch causes repetition of the operations initiated by pressing CONTINUE, EXAMINE NEXT, or DEPOSIT NEXT keys as long as the key is held on. The SPEED controls govern the rate of repetition. The indicator lights to denote activation of the REPEAT controls.
POWER switch and indicator	This switch controls the application of primary power to the computer and to all its attached external devices. When power is on, the indicator lights.
ACCUMULATOR switches	Used to establish the 18-bit word to be placed in core memory by the DEPOSIT and DEPOSIT NEXT keys, or the word to be placed in the AC by a program. These switches are also used for program sense control.
ADDRESS switches	Used to establish the 15-bit core memory address loaded into the PC by operation of the START, EXAMINE, or DEPOSIT keys.
MULTIPLIER QUOTIENT indicators*	Display the contents of the MQ.
ACCUMULATOR indicators	Display the contents of the AC.
MEMORY BUFFER indicators	Display the contents of the MB.
MEMORY ADDRESS indicators	Display the contents of the MA.

*These indicators function only when the computer is equipped with a Type 177 Extended Arithmetic Element option.

TABLE 2-1 OPERATOR CONSOLE CONTROLS AND INDICATOR (continued)

Control or Indicator	Function
PROGRAM COUNTER indicators	Display the contents of the PC.
LINK indicator	Display the contents of the link.
PIE indicator	Lights when the program interrupt is enabled.
RUN indicator	Lights when the computer is executing instructions.
FETCH, DEFER, EXECUTE, BREAK indicators	Light to display the major control state of the next memory cycle.

2.2.2 Indicator Panel

The Indicator Panel is shown in figure 2-2 and indicators are listed in table 2-2.

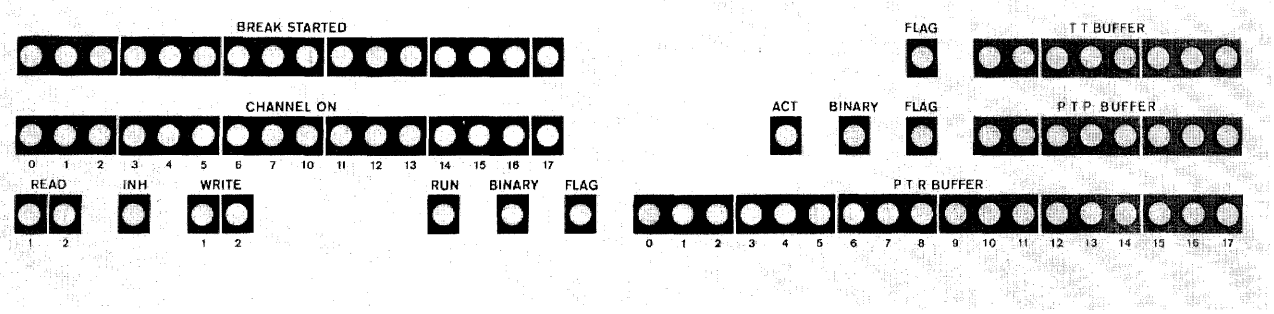


Figure 2-2 Indicator Panel

TABLE 2-2 INDICATOR PANEL FUNCTIONS

Indicator	Function
READ 1,2	Designate the status of timing control flip-flops in the memory control and indicate that the core memory is in a read cycle.
INH	Designates the status of the INH (inhibit) flip-flop in the memory control and indicates the memory is in a write cycle.
WRITE 1,2	Designate the status of timing control flip-flops in the memory control and indicate that the core memory is in a write cycle.
CHANNEL ON	Lighted indicators denote enabled priority interrupt channels of the Type 172 Automatic Priority Interrupt.
BREAK STARTED	Lighted indicators denote program interrupt channels that are active (requesting or using a break cycle).
RUN	Denotes the status of the RUN flip-flop in the Type 444B Perforated Tape Reader and Control, and indicates operation of this device.
BINARY (bottom row)	Lights to designate that the perforated tape reader is in the binary mode. If this lamp is not lit, the reader is in the alphanumeric mode.
FLAG (bottom row)	Denotes the status of the perforated tape reader flag.
PTR BUFFER	Indicates the contents of the data buffer register of the perforated tape reader (last character or binary word read).
ACT	Denotes the active or operating status of the Type 75D Perforated Tape Punch and Control.
BINARY (center row)	Lights to designate that the perforated tape punch is in the binary mode.
FLAG (center row)	Denotes the status of the perforated tape punch flag.

TABLE 2-2 INDICATOR PANEL FUNCTIONS (continued)

Indicator	Function
PTP BUFFER	Indicates the contents of the data buffer register of the perforated tape punch (last character punched).
FLAG (top row)	Denotes the status of the Type 649 Teleprinter and Control line unit in (TTY) flag. (The in direction is referenced to the computer, not to the Teletype equipment.)
TT BUFFER	Indicates the contents of the Teletype control line unit in (TTY) data register (code of the last keyboard character struck).

2.2.3 Perforated Tape Reader Controls

The tape reader appears in figure 2-3. Table 2-3 lists the tape reader controls and explains their functions.

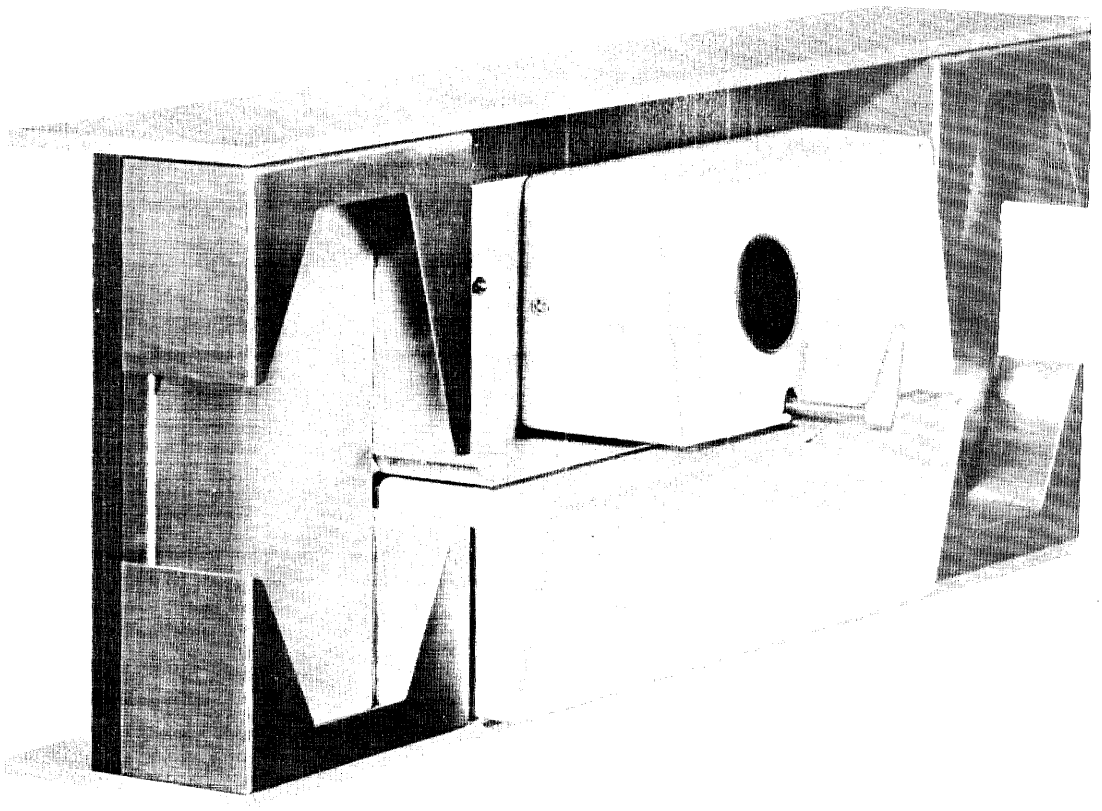


Figure 2-3 Perforated Tape Reader

TABLE 2-3 TAPE READER CONTROLS

Control	Function
POWER ON switch	Applies power to the power supply, capstan drive motor, and fan motor.
READY/LOAD switch and Tape width selector knob	In its clockwise position, the READY/LOAD switch de-energizes the brake and pinch roller to allow tape insertion. The knob may be moved in or out to handle different tape levels.

2.2.4 Teletype Controls

The Teletype appears in figure 2-4. Table 2-4 lists the Teletype controls and explains their functions.

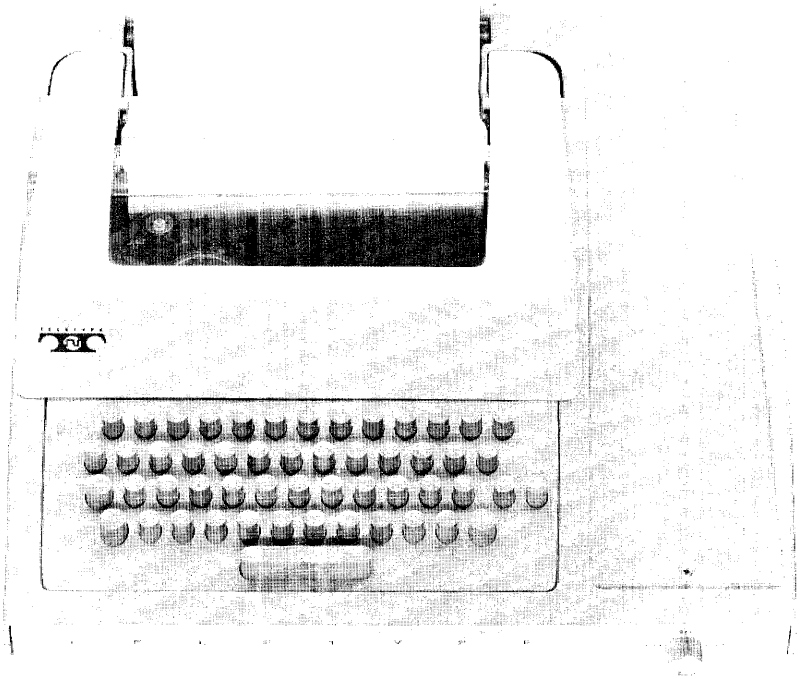


Figure 2-4 Teletype Console

TABLE 2-4 TELETYPE CONSOLE CONTROLS

Control	Function
KEYBOARD	Provides a means of supplying input data, in the form of typed characters, to the computer and/or the page printer, depending on the setting of the LINE/OFF/LOCAL switch.
LINE/OFF/LOCAL switch	Controls the application of primary power to the Teletype and controls data connection between the Teletype and the central processor. In the LINE position, the Teletype is energized and connected as an I/O device of the computer. In the OFF position, the Teletype is de-energized. In the LOCAL position, the Teletype is energized for off-line operations, and the signal connections to the processor are broken. Both line and local use of the Teletype requires that the computer be energized through the POWER switch.

2.3 OPERATING PROCEDURES

Several methods are available for loading and unloading PDP-7 information. The method used is dependent upon the form of the information, time limitations, and the peripheral equipment connected to the computer. The following procedures are basic to any use of the PDP-7, and although they may be used infrequently later on, they are valuable in preparing the initial programs and learning the function of machine input and output transfers.

2.3.1 Manual Data Storage and Modification

The use of the facilities on the operator console permits manual storage or modification of programs and data. Chief use of the manual data storage facilities is to load the Readin Mode Loader program and all other programs in read-in mode format into the computer core memory.

The Readin Mode (RIM) Loader is a program used to automatically load programs into PDP-7 from perforated tape in RIM format. This program and the RIM tape format are described in the PDP-7 User Handbook F-75A and in Digital Program Library descriptions. The RIM program is listed in table 2-5 for rapid reference and can be used as an exercise in manual data storage. To store data manually in the PDP-7 core memory:

a. Turn the lock switch counterclockwise and set the POWER switch to the up position.

b. Set the ADDRESS switches to correspond with the address of the first word to be stored. (In the case of the RIM loader program, this is 17762_8).

NOTE: Whenever an address in core memory is given in this section, it is intended to apply to an 8K memory. To translate this to the correct 4K memory address, subtract 10000_8.

c. Set the ACCUMULATOR switches to correspond with the binary contents of the first word. (In the case of the RIM Loader program, this is zero.)

d. Momentarily lift the DEPOSIT/DEPOSIT NEXT key to deposit the word in memory.

e. Note the contents of the four storage registers (AC, MB, MA, and PC) as given by their respective indicators after completion of the deposit operation. The AC and MB must both contain the data word just deposited, the MA must contain the address of the core memory cell in which the word was deposited, and the PC must contain the address of the next consecutive core memory cell (MA+1).

f. Store all additional data words by momentarily depressing the DEPOSIT/DEPOSIT NEXT key to the DEPOSIT NEXT position after each successive data word has been set in the ACCUMULATOR switches. The contents of the PC will be incremented by 1 during each deposit next operation, thus setting up the address of the core memory cell used for the next operation. The RIM Loader contains the following program:

TABLE 2-5 READIN MODE (RIM) LOADER PROGRAM

Address (octal)	Content (octal)	Tag	Mnemonic	Comments
17762/	0	R,	0	/READ ONE BINARY WORD
17763/	700101		RSF	
17764/	617763		JMP .-1	/WAIT FOR WORD TO COME IN
17765/	700112		RRB	/READ BUFFER
17766/	700144		RSB	/READ ANOTHER WORD
17767/	637762		JMP I R	/EXIT SUBROUTINE
17770/	700144	GO,	RSB	/ENTER HERE, START READER /GOING

TABLE 2-5 READIN MODE (RIM) LOADER PROGRAM (continued)

Address (octal)	Content (octal)	Tag	Mnemonic	Comments
17771/	117762	G,	JMS R	/GET NEXT BINARY WORD
17772/	057775		DAC OUT	
17773/	417775		XCT OUT	/EXECUTE CONTROL WORD
17774/	117762		JMS R	/GET DATA WORD
17775/	0	OUT,	0	/STORE DATA WORD
17776/	617771		JMP G	/CONTINUE

g. To recheck a loaded program, set the ADDRESS switches to the starting address and momentarily set the EXAMINE/EXAMINE NEXT key to the EXAMINE position. After the first cell has been checked, the remaining cells may be examined in sequence simply by repeatedly setting the switch to the EXAMINE NEXT position without adjusting the ADDRESS switches. By repeating steps b through d using the address of the cell in question, it is possible to alter the contents of any cell.

2.3.2 Loading Binary Data Using READ-IN Key

Binary format tapes (including the RIM Loader tape) can be loaded directly into the computer without the need of a prestored program, as follows:

a. Turn the computer lock switch counterclockwise and set the POWER switch to the up position.

b. Set the tape reader POWER ON switch to ON.

c. Set the READY/LOAD switch to LOAD (clockwise) and insert the binary tape. The tape is placed in the right-hand loading bin of the reader, and, during reading, travels to the left-hand bin. When the tape is properly positioned, there will be three bit positions to the rear of the sprocket wheel and five bit positions to the front.

d. Set the tape reader READY/LOAD switch to READY.

e. Set up the starting address of the tape (found on the leader) on the ADDRESS switches.

f. Press and release the computer READ-IN key. The tape will be read automatically.

2.3.3 Loading Data Under Program Control

Information (in other than binary format) can be stored or modified in the computer automatically only by executing programs previously stored in memory. For example, having the RIM Loader stored in the core memory allows the loading of RIM format tapes as follows:

a. Turn the computer lock switch counterclockwise and set the POWER switch to the up position.

b. Set the tape reader POWER ON switch to ON.

c. Set the READY/LOAD switch to LOAD and insert the tape into the tape reader.

d. Using the ADDRESS switches, set the starting address of the RIM Loader program (17770).

e. Press and release the computer START key.

f. Press the START key. The tape is read automatically. The program contained on the tape may be initialized and started automatically after being loaded. This occurs because some tapes in RIM format are concluded with address 0000 and a data word equal to one less than the starting address of the program just read. Therefore, after the last tape character is read, the program starting address is taken by the program counter as the address of the next instruction to be executed.

2.3.4 Assembling Programs

Programs prepared in binary format and written in symbolic language can be assembled into binary, machine-language program tapes as described in appropriate Digital Program Library documents, as follows:

a. Turn the lock switch counterclockwise and set the POWER switch to the on (up) position.

b. Set the tape reader POWER ON switch to ON.

c. Store the RIM Loader program, either manually or by use of the READ-IN key, as previously described.

d. Load the assembler program by means of the assembler tape. Since the assembler tape is in RIM format, it can be loaded by the method described in paragraph 2.3.3. When the tape has been run, the AC should contain all 0s. If it does not, a checksum error has been detected; showing improper storage of the program. When this occurs, the tape must be rerun until the AC does finally contain all 0s at the conclusion of the loading process, indicating proper storage of the program. Repeated errors indicate defects in either the assembler tape or the PDP-7 system.

e. Set the tape reader READY/LOAD switch to the LOAD position, and insert the symbolic language tape to be converted into machine-language, binary format, into the tape reader. Put switch back to READY position.

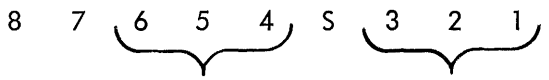
f. Put the starting address of the assembler program (0020) into the ADDRESS switches of the operator console. (Set ACCUMULATOR switch 10 up to indicate ASCII, or down to indicate FIODEC.)

g. Press and release the CONTINUE key.

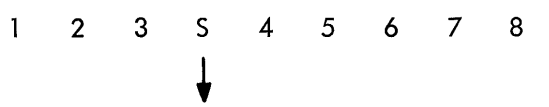
h. When assembly is complete, the assembler will stop with all 1s in the AC.

2.3.5 Teletype Code

The 8-bit code used by the Model 33 KSR Teletype unit is the American Standard Code for Information Interchange (ASCII) modified. This code is read in the reverse of the normal octal form used in the PDP-7 since bits are numbered from right to left, from 1 through 8, with bit 1 having the most significance. Therefore, perforated tape is read:



Tape is loaded into the reader:



The Model 33 KSR set can generate all assigned codes except 340 through 374 and 376. Generally, codes 207, 212, 215, 240 through 337, and 377 are sufficient for Teletype operation. The Model 33 KSR ser can detect all characters, but does not interpret as commands all of the codes that it can generate. The standard number of characters printed per line is 72. The sequence for proceeding to the next

line is a carriage return followed by a line feed (as opposed to a line feed followed by a carriage return). Key or key combinations required to produce octal codes from 200 through 337, 375, and 377 are indicated in table 2-6 with the associated ASCII character.

TABLE 2-6 TELETYPE CODE

Octal Code	Character Name	ASCII Character	Teletype Character	Key or Key Combinations
200	Null/Idle	NULL	---	CTRL @
201	Start of Message	SOM	---	CTRL A
202	End of Address	EOA	---	CTRL B
203	End of Message	EOM	---	CTRL C
204	End of Transmission	EOT	---	CTRL D
205	Who Are You	WRU	---	CTRL E
206	Are You	RU	---	CTRL F
207	Audible Signal	BELL	---	CTRL G
210	Format Effector	FE	---	CTRL H
211	Horizontal Tabulation	H TAB	---	CTRL I
212	Line Feed	LF	---	CTRL J
213	Vertical Tabulation	V TAB	---	CTRL K
214	Form Feed	FF	---	CTRL L
215	Carriage Return	CR	---	CTRL M
216	Shift Out	SO	---	CTRL N
217	Shift In	SI	---	CTRL O
220	Device Control Reversed for Data Line Escape	DC0	---	CTRL P
221	Device Control On	DC1	---	CTRL Q
222	Device Control (TAPE)	DC2	---	CTRL R
223	Device Control Off	DC3	---	CTRL S
224	Device Control ~~(TAPE)~~	DC4	---	CTRL T
225	Error	ERR	---	CTRL U
226	Synchronous Idle	SYNC	---	CTRL V
227	Logical End of Media	LEM	---	CTRL W
230	Separator, Information	S0	---	CTRL X
231	Separator, Data Delimiters	S1	---	CTRL Y
232	Separator, Words	S2	---	CTRL Z

TABLE 2-6 TELETYPE CODE (continued)

Octal Code	Character Name	ASCII Character	Teletype Character	Key or Key Combinations
233	Separator, Groups	S3	---	SHIFT CTRL K
234	Separator, Records	S4	---	SHIFT CTRL L
235	Separator, Files	S5	---	SHIFT CTRL M
236	Separator, Misc.	S6	---	SHIFT CTRL N
237	Separator, Misc.	S7	---	SHIFT CTRL O
240	Space	SP	Space	Space Bar
241	Exclamation Point	!	!	SHIFT !
242	Quotation Marks	"	"	SHIFT "
243	Number Sign	#	#	SHIFT #
244	Dollar Sign	$	$	SHIFT $
245	Percent Sign	%	%	SHIFT %
246	Ampersand	&	&	SHIFT &
247	Apostrophe	'	'	SHIFT '
250	Parenthesis, Beginning	(	(	SHIFT (
251	Parenthesis, Ending	)	)	SHIFT)
252	Asterisk	*	*	SHIFT *
253	Plus Sign	+	+	SHIFT +
254	Comma	,	,	,
255	Hyphen	-	-	-
256	Period	.	.	.
257	Virgule	/	/	/
260	Numeral 0	0	0	0
261	Numeral 1	1	1	1
262	Numeral 2	2	2	2
263	Numeral 3	3	3	3
264	Numeral 4	4	4	4
265	Numeral 5	5	5	5
266	Numeral 6	6	6	6
267	Numeral 7	7	7	7
270	Numeral 8	8	8	8
271	Numeral 9	9	9	9

TABLE 2-6 TELETYPE CODE (continued)

Octal Code	Character Name	ASCII Character	Teletype Character	Key or Key Combinations
272	Colon	:	:	:
273	Semicolon	;	;	;
274	Less Than	<	<	SHIFT <
275	Equals	=	=	SHIFT =
276	Greater Than	>	>	SHIFT >
277	Interrogation Point	?	?	SHIFT ?
300	At	@	@	SHIFT @
301	Letter A	A	A	A
302	Letter B	B	B	B
303	Letter C	C	C	C
304	Letter D	D	D	D
305	Letter E	E	E	E
306	Letter F	F	F	F
307	Letter G	G	G	G
310	Letter H	H	H	H
311	Letter I	I	I	I
312	Letter J	J	J	J
313	Letter K	K	K	K
314	Letter L	L	L	L
315	Letter M	M	M	M
316	Letter N	N	N	N
317	Letter O	O	O	O
320	Letter P	P	P	P
321	Letter Q	Q	Q	Q
322	Letter R	R	R	R
323	Letter S	S	S	S
324	Letter T	T	T	T
325	Letter U	U	U	U
326	Letter V	V	V	V
327	Letter W	W	W	W
330	Letter X	X	X	X

TABLE 2-6 TELETYPE CODE (continued)

Octal Code	Character Name	ASCII Character	Teletype Character	Key or Key Combinations
331	Letter Y	Y	Y	Y
332	Letter Z	Z	Z	Z
333	Bracket, Left	[	[	SHIFT K
334	Reverse Virgule	\	\	SHIFT L
335	Bracket, Right	]	]	SHIFT M
336	Up Arrow (exponentation)	↑	↑	↑
337	Left Arrow	←	←	SHIFT ←
340 through 374 are not available				
375	Unassigned Control	(1)	---	ALT MODE
376	Not Available			
377	Delete/Idle/Rub Out	DEL	---	RUB OUT

2.3.6 Local Teletype Operation

The Teletype can be used as an ordinary typewriter as follows:

a. Set the computer lock switch to the counterclockwise position.

b. Set the computer POWER switch to the up position.

c. Set the Teletype LINE/OFF/LOCAL switch to the LOCAL position.

d. Type out the desired information on the Teletype keyboard.

2.4 PROGRAMMING

2.4.1 The Programming System

Programming instructions are to be found in chapter 3 and the PDP-7 User Handbook. Refer to the User Manual for detailed programming procedures.

2.4.2 Maintenance Programs

The basic maintenance routines for PDP-7 are:

Teleprinter I/O Test

Clock Interrupt Test

Reader and Punch Test

Maindec 710 (RPB Test)

Maindec 701 (Instruction Test)

Maindec 703 (Memory)

Maindec 702 (Address Test)

Contest II

(See Program Library List)

The first four are primarily input/output system tests; while the Maindec routines are processor and memory system checks. Refer to specific write ups in PDP-7 Program Library for detailed descriptions.

These routines are diagnostic programs designed to test specific functions within the computer system. Maindec routines are available as perforated paper tapes in hardware readin mode (HRI) format. Each diagnostic routine tape is accompanied by a description of the program, procedures for using the program, and information on analyzing the program results to locate specific failures. Applications of these routines are indicated at the appropriate points in chapter 5 as they apply to preventive or corrective maintenance of the PDP-7 system. To execute these routines the user should be familiar with the machine programming described in the User Handbook.

CHAPTER 3
SYSTEM DESCRIPTION

3.1 FUNCTIONAL DESCRIPTION

The major functional units of the PDP-7 are the central processor, the memory, and the I/O devices. The central processor performs arithmetic or logical operations upon data stored in memory and controls the operation of the I/O devices. A series of instructions stored in memory, or the manipulation of keys and switches on the operator console determines the nature and sequence of these operations. During programmed operation, the processor retrieves from memory the instruction specified by the program, executes the instruction during one or more computer cycles, and then proceeds to retrieve and execute the remaining instructions specified by the program sequence. All arithmetic, logical, and control operations are performed as a function of three factors: the instruction retrieved from memory; the major control state established by the instruction; and the timing pulses produced by the processor. During manual operation, the operator controls are used to stop and start programmed operation, to manually select and examine specific memory locations, and to select special operating modes.

3.1.1 Instructions

Instructions are of two types: memory reference and augmented. All instructions contain an operation code (specifying the nature of the instruction) in bits 0 through 3.

Memory reference instructions cause information to be stored in or retrieved from memory, and contain a memory address as well as an operation code. All memory reference instructions require one computer cycle in which the instruction is retrieved, and all except the jump instruction require a second cycle in which to execute the instruction specified by the operation code. The jump does not cause storage or retrieval of information, but transfers control of the processor from one block of consecutive memory locations (containing instructions) to a different block of consecutive locations. The jump instruction is normally completed in one computer cycle. If indirect addressing is employed, two cycles are required for the jump and three cycles for other memory reference instructions.

Augmented instructions do not require reference to memory. Since no address is required, bits 4 through 17 are decoded to initiate various operations to extend or augment the operation code. Because no storage or retrieval operations are performed, most augmented instructions can be completed in one computer cycle. Augmented instructions are divided into three classes:

a. Instructions having an operation code of 64_8 are EAE instructions.

b. Instructions having an operation code of 70_8 are input/output transfer (IOT) commands, and are used to control or test the status of I/O devices, or to effect an information transfer.

c. Instructions having an operation code of 74_8 are operate (OPR) commands, and are used for basic processor data manipulation such as instruction skipping as a function of register condition, shifting, rotating, etc.

The formats of the various types of instruction words are illustrated in figure 3-1. Table 3-2 contains a list of the instructions performed by the PDP-7.

3.1.2 Major Control States

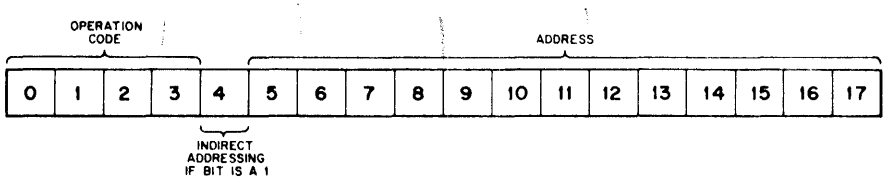
The computer operates in one of four major control states during each machine timing cycle. One or more states are entered to execute an instruction. The states are fetch, execute, defer, and break and are determined by the major state generator. Only one state exists at a time and all states, except break, are determined by the programmed instruction being executed.

3.1.2.1 Fetch (F) - A new instruction is obtained when this state is entered. The contents of the memory cell specified by the PC are placed in the MB, and the operation code (bits 0-3) of this instruction word is placed in the IR. The contents of the PC are then incremented by 1. If a single-cycle instruction is fetched, the operations specified are performed during the last part of the fetch cycle; then the next cycle is a fetch state for the next instruction. If a 2-cycle instruction is fetched, the succeeding control state is either defer or execute.

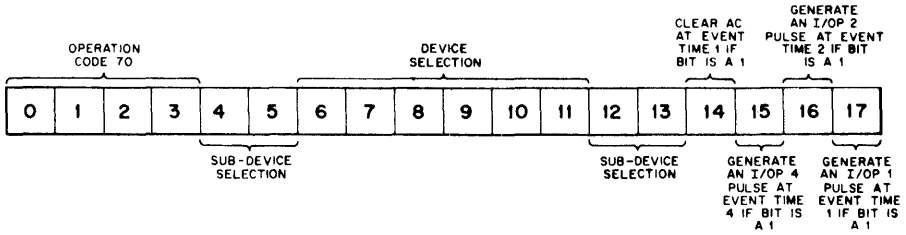
3.1.2.2 Defer (D) - When bit 4 of a memory reference instruction is a 1, the defer state is entered following the fetch state, to perform the indirect addressing. The memory location addressed by the instruction contains the address of the operand, and access to the operand is deferred to the next memory cycle (execute).

3.1.2.3 Execute (E) - This state is established only when a memory reference instruction is being executed. The contents of the memory cell addressed are brought into the MB, and the operation specified by the contents of the IR is performed.

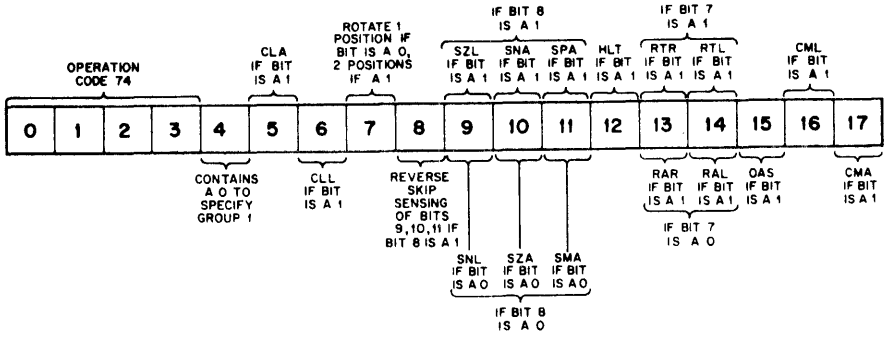
3.1.2.4 Break (B) - When this state is established, the sequence of instructions is broken for a data interrupt or a program interrupt. In both cases, the break occurs only at the completion of the current instruction. The data break interrupt allows for the transfer of information between core memory and an external device. When this transfer has been completed, the program sequence is resumed from the point of the break. The program interrupt causes the sequences to be altered. The contents of the PC and the contents of the link are stored in core memory location 0000, and the program continues from location 0001.



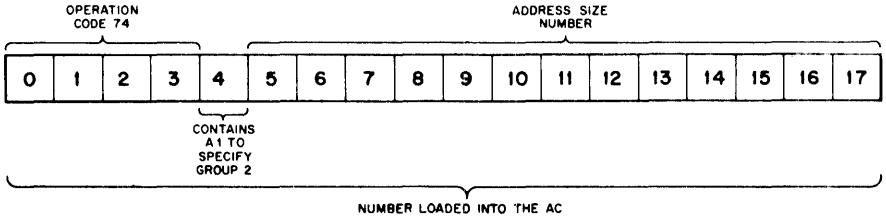
Memory Reference Instruction Bit Assignments



IOT Instruction Bit Assignments



Group 1 Operate Instruction Bit Assignments



Group 2 (LAW) Operate Instruction Bit Assignments

Figure 3-1 Instruction Word Format

3.1.3 Timing

Seven times (designated T1 through T7) occur in sequence during each computer cycle. At each time, two pulses are generated, one of which is 40 nsec and the other 70 nsec wide. These time pulses cause gating circuits to perform sequential or synchronized logical or control operations. The narrow pulses are used for operations where timing is critical, such as the simultaneous sampling and incrementing of a register; the wider pulses are used to initiate gating operating where timing is less critical. The intervals between successive pairs of timing pulses permit gates and registers to settle before initiating a new operation. During each computer cycle, memory reading occurs between times T2 and T3; memory writing starts at time T4 and occupies the remaining portion of the cycle.

3.2 LOGIC FUNCTIONS

Both manual and programmed operation of the PDP-7 are required for the performance of any complete task. Manual operation is normally limited to the following: storing a brief loader program; modifying or examining data or addresses in a program already stored; or establishing the starting conditions for programmed operation. In programmed operation, data and the sequence of instructions which constitutes the program are loaded into the core memory; the starting address of the program is manually established; and the computer is manually started. The computer then successively executes the instructions specified by the program. For maintenance purposes and to facilitate debugging, there is provision for advancing the program one cycle or one instruction at a time.

3.2.1 Flow Diagram Interpretation

Two flow diagrams are provided: one, contained in engineering drawing 3, shows the events that take place during each of the possible manual operations; the other, contained in engineering drawing 4, shows the events that take place during the execution of instructions. The two flow diagrams, similar in their arrangement, at the extreme left, show the timing pulses which initiate events at various times in the cycle. In the flow diagram of manual operations, these timing pulses are designated KEY MANUAL and SP0 through SP4. In the flow diagram of programmed operations, the timing pulses are designated T1 through T7. Times (in μsec or nsec), appearing in boxes that straddle the horizontal boundary line separating two timing pulses, represent the time interval lapse between occurrence of those two pulses.

Events initiated by a specific timing pulse appear in rectangular boxes placed between boundary lines associated with that pulse. It is important to note that all such events are initiated simultaneously by the timing pulse if they form part of the event sequence. For example, in following the deposit (DP) sequence on engineering drawing 3 at time SP2 the event AS1 → PC is followed in the sequence by DAC→ IR and ACS1 → AC. The vertical separation does not imply that the AS1 → PC operation precedes the

other two; on the contrary, they are all initiated simultaneously. The vertical separation merely facilitates the illustration of branches to other possible sequences.

Events in a sequence which is not specifically designated by a key name or instruction name are assumed to be common to all sequences (e.g., 0 → MA at time SP1, engineering drawing 3). Where a common sequence branches into two or more sequences, depending on the operation in progress, the operation associated with a given sequence is identified immediately below the branch. For example, at time SP2 the event AS1 → PC occurs in a sequence common to both examine (EX) and deposit (DP) operations. The sequence then branches. If an examine operation is in progress, pulse SP2 initiates the event LAC → IR, but if a deposit operation is in progress, LAC → IR does not occur. Instead, pulse SP2 initiates events DAC → IR and ACS1 → IR. Similarly, a common sequence may follow several separate sequences. Thus, on engineering drawing 4, each of the separate sequences associated with the START, CONTINUE, EXAMINE, and DEPOSIT operations is followed by the event 1 → TP1 which takes place at time SP4.

Note that some of the events specified in the rectangles of the flow diagram are unconditional; that is, they invariably occur at the specified time when the operation with which they are associated is in progress. Thus, when the START key is pressed, the event AS1 → PC always takes place at time SP2. Other events are conditional upon the state of control flip-flops or register bits. Conditional events are represented in the rectangles by a statement of the required condition, which is separated from the conditional event by a colon. Thus, at time SP2 of a readin operation (engineering drawing 3), the statements in the rectangle indicate that if the read paper tape (RPT) flip-flop is in the 0 state, the contents of the address switch register are transferred to the PC (RPT (0): AS1 → PC). However, if the RPT flip-flop is in the 1 state, 1 is added to the contents of the PC and the operation code DAC (deposit content of accumulator in specified memory cell) is set into the instruction register (RPT (1): + 1 → PC DAC → IR).

On engineering drawing 4, the seven time pulses that occur during each computer cycle appear at the left. The column immediately to the right contains the events associated with memory which occur during every computer cycle, regardless of the major control state established. This column, designated Events Common, also contains certain conditional events, whose occurrence is dependent on factors other than the major state. The other events on this drawing are grouped according to the major state established. Each major state (fetch, defer, execute, and break) lasts for one computer cycle, and all start in the fetch state.

The exact mechanism by which the CP performs a function specified by an event shown on the flow diagram is found by referring to the appropriate engineering logic diagram and the corresponding circuit description. When tracing a transfer function, it is best to begin by examining the input and control gating of the register to which the transfer is being made. Thus, to trace the function AS1 → PC, first examine the logic diagram of the PC, which shows that a set of input gates is triggered by a pulse

designated AS1 → PC. To find out how this pulse is generated, examine the logic drawing of the PC control. When there is doubt as to where a pulse or level is generated, consult chapter 6. This chapter lists all command pulses and control levels in alphanumerical order of their designations, together with the number of the engineering logic diagram on which are shown the circuits which generate any given signal.

3.2.2 Preliminary Operations

The circuit breaker mounted on the 2-step power control unit located at the rear of the cabinet governs circuit protection and primary control of all power entering the computer. The lock switch and POWER switch located on the console panel governs manual control of primary power. With the lock switch in the unlocked position, turning on the POWER switch energizes a relay in the power control unit, which in turn immediately energizes the computer logic power supply. A second relay in the power control unit imposes a delay of 5 sec before the memory power supply is energized. This delay ensures that all ac transients in the computer have completely decayed before the memory is energized. Similarly, when the POWER switch is turned off, the memory power supplies are de-energized immediately and the computer logic power is maintained for 5 sec longer. In each case, the delay ensures that switching transients cannot cause current surges thereby destroying information stored in the core memory.

During the 5-sec turn-on delay period, an integrating circuit enables a variable clock. While the clock is enabled, it emits standard negative pulses at a repetition rate of 200 kc. These PWR CLK (power clock) pulses repeatedly clear the RUN and memory control flip-flops and trigger two NAND gates, which the 0 condition of the RUN flip-flop enables. The output pulses from the gates trigger two pulse amplifiers, which produce the PWR CLR NEG (power clear negative) and PWR CLR POS (power clear positive) pulses. These PWR CLR pulses are supplied to the interface to establish initial conditions in peripheral equipment. Thus, if switching transients set any flip-flops during the first 5 sec after power turn-on, the PWR CLK or PWR CLR pulses immediately clear them. This establishes correct initial conditions and ensures that a stored program cannot be accidentally started or disturbed.

The lock switch, in its unlocked position, connects all the console keys and switches to the −15v supply, thereby permitting them to generate the levels required to start the computer and to perform manual operations. When a program has been started manually, the lock switch may be turned to its locked position. This grounds all the console keys and switches to prevent manual interference with the program. A second deck of the lock switch bypasses the POWER switch, so that power cannot be accidentally turned off while a program is running.

3.2.3 Manual Operations

Keys and switches on the operator console have three functions: they permit the storing of information in core memory; they permit the contents of a specified core memory cell to be displayed for visual examination; and they permit the starting and stopping of execution of a program.

Operation of the START, CONTINUE, EXAMINE/EXAMINE NEXT, DEPOSIT/DEPOSIT NEXT, or READ-IN keys generates the KEY MANUAL level transition to start the special pulse generator. The special pulse generator produces five timing pulses, designated SP0 through SP4, which initiate all functions performed as part of a manual operation. All five keys cause the RUN flip-flop to be cleared at time SP0 in order to stop any operations already in progress. (Note that although it is not logical to press the START key when a program is running, it could be accidentally pressed and must therefore be made to stop current operations.) After the clearing of the RUN flip-flop, there is a 10-μsec pause to allow the completion of any EAE operations in progress. Thereafter, the sequence of operations depends upon which key was operated.

3.2.3.1 START Key - The START key initiates execution of a program previously loaded into memory. After starting the special pulse generator and clearing the RUN flip-flop, the key causes the following events to take place:

a. At time SP1, the memory address register (MA) is cleared in preparation for entering the starting address of the program from the ADDRESS switches. A complete clear is required, because only binary 1s are transferred to the MA.

b. At time SP1, a BGN pulse is generated which clears the instruction register (IR), the read paper tape (RPT) and other special mode flip-flops, and establishes initial conditions in the registers of I/O devices. The multistate device of the major state generator is forced into the fetch state in preparation for extracting the first programmed instruction from memory, and the program counter (PC) is cleared.

c. At time SP2 , binary 1s of the starting address preset on the ADDRESS switches are transferred into the PC.

d. At time SP3, the RUN flip-flop is set to the 1 state, thereby conditioning a NAND gate between the special pulse generator and the main timing chain. Timing pulse SP4 triggers this gate and causes the main timing chain to generate timing pulse T1. Thereafter, the CP operates under control of timing pulses generated by the main timing chain and successively executes programmed instructions until the RUN flip-flop is set to the 0 state.

3.2.3.2 CONTINUE Key - The CONTINUE key causes the CP to continue execution of a program after a temporary halt. Pressing the key clears the RUN flip-flop during SP0 and the MA during SP1. Since a halt may take place at the end of any memory cycle, the CP must continue with the type of cycle that was predetermined by the cycle in which the halt was requested. Thus, the only further action required by the CONTINUE key is to set the RUN flip-flop to 1 at time SP3 and to cause timing pulse SP4 to initiate operation of the main timing chain. The CP then continues execution of the program from the point at which it was halted.

3.2.3.3 STOP Key - The STOP key provides a means of halting a program at the conclusion of a memory cycle. Pressing the key conditions a gate triggered at time T5 of the memory cycle. The output pulse produced by the gate clears the RUN flip-flop, thereby preventing timing pulse TP7 from reentering the timing chain to initiate a new cycle. The CP, therefore, halts at the conclusion of the memory cycle during which the RUN flip-flop was cleared.

3.2.3.4 DEPOSIT/DEPOSIT NEXT Key - The DEPOSIT/DEPOSIT NEXT key, when momentarily set to DEPOSIT, causes a binary number that has been preset on the ACCUMULATOR switches to be deposited in the memory cell specified by the ADDRESS switches. When momentarily set to DEPOSIT NEXT, the key causes a binary number preset on the ACCUMULATOR switches to be deposited in the memory cell specified by the PC. Setting the key to DEPOSIT clears the RUN flip-flop at time SP0 and the MA at time SP1. A memory cycle to perform the operation is then initiated as follows:

a. At time SP1, a BGN pulse is generated to clear special mode and I/O device flip-flops; the PC is cleared; and the major state generator is forced to the execute state. (Refer to the key function flow diagram on engineering logic diagram 3.)

b. At time SP2, the binary 1s contained in the ADDRESS switches are transferred to the PC. Then the binary 1s contained in the ACCUMULATOR switches are transferred to the accumulator register (AC), and the operation code for DAC (deposit AC) is set into the IR.

c. At time SP3, the contents of the PC are transferred into the MB. This step is necessary because after time SP4, the processor enters an execute cycle in which the contents of the MB are transferred to the MA at time T1. The fact that the status of the link, trap flag, and extend mode are also set into the MB is of no importance in a deposit operation, because the MA does not sample those bits of the MB.

d. At time SP4, the contents of the PC are incremented by 1 to facilitate a further manual operation at the next location after completing the deposit operation. Timing pulse SP4 then

starts the main timing chain. Note that the RUN flip-flop remains in the 0 state, and consequently the CP halts at the end of the execute cycle.

e. At time T1 of the execute cycle, since this is not a CAL (call subroutine) instruction, the contents of the MB are transferred to the MA (CP flow diagram, engineering logic diagram 4).

f. At time T3 of the execute cycle the contents of the AC are transferred to the MB; and during the remaining portion of the cycle this data is written into the specified memory cell. Since the RUN flip-flop is not set, the CP halts after time T7 and the deposit operation is complete.

Setting the key to DEPOSIT NEXT causes the CP to perform an operation that is almost identical to a deposit operation. The difference is that the PC is not cleared at SP1, nor are the contents of the ADDRESS switches set into the PC at time SP2. The number preset on the ACCUMULATOR switches is therefore deposited in the memory cell specified by the PC instead of by the ADDRESS switches. Note that the contents of the PC are incremented at time SP4. Therefore, after an initial deposit operation, use of the DEPOSIT NEXT position causes deposits to be made at consecutive memory locations without resetting the ADDRESS switches.

3.2.3.5 EXAMINE/EXAMINE NEXT Key - The EXAMINE/EXAMINE NEXT key, when momentarily set to EXAMINE, causes the contents of the memory cell specified by the ADDRESS switches to be transferred to the MB and AC. When the transfer is complete, the associated indicator lamps display the contents of the MB, MA, and AC. The MB and AC contain the contents of the specified memory cell; the MA contains the address preset on the ADDRESS switches; and the PC contains the address of the next consecutive memory cell. Thus, a number of consecutive memory cells may be examined without resetting the ADDRESS switches between each operation. When momentarily set to EXAMINE NEXT, the key causes the contents of the memory cell specified by the PC to be transferred to the AC for visual examination.

Setting the key to EXAMINE clears the RUN flip-flop during time state SP0 and the MA at time SP1. A memory cycle to perform the operation is initiated as follows:

a. At time SP1, a BGN pulse is generated to clear special mode and I/O device flip-flops; the PC is cleared; and the major state generator is forced to the execute state. (Refer to the key function flow diagram on engineering logic diagram 3.)

b. At time SP2, the address specified by the ADDRESS switches is transferred to the PC, and the operation code for LAC (load AC) is set into the IR.

c. At time SP3, the contents of the PC are transferred to the MB. (This step is necessary for the reason stated under 3.2.3.4 c.

d. During time state SP4, the contents of the PC are incremented by 1, and timing pulse SP4 starts the main timing chain.

e. At time T1 of the execute cycle, since the instruction is not CAL, the address contained in the MB is transferred to the MA, and the AC is cleared.

f. At time T3, the contents of the addressed memory cell are read into the MB, and an XOR (exclusive OR) operation is performed on the MB and AC. Since the AC was previously cleared, this results in a direct transfer of the contents of the MB into the AC, where they are available for visual examination. Since the RUN flip-flop is not set, the CP halts at time T7, and the EXAMINE operation is complete.

Setting the key to EXAMINE NEXT causes the CP to perform an operation almost identical to an EXAMINE operation. The difference is that the PC is not cleared at time SP1, nor are the contents of the ADDRESS switches set into the PC at time SP2. The word loaded into the AC for examination is therefore brought from the cell specified by the PC instead of by the ADDRESS switches. Note that the contents of the PC are incremented at time SP4 to permit examination of consecutive locations without resetting the ADDRESS switches.

3.2.3.6 REPEAT Switch - Turning on the REPEAT switch causes the CP to repeat the operation specified by one of the manual keys, at intervals determined by the setting of the SPEED controls on the console panel, for as long as the key is held down. After completing a DEPOSIT or EXAMINE operation, use of the REPEAT switch in conjunction with a DEPOSIT NEXT or EXAMINE NEXT operation permits deposition in, or examination of, successive memory cells without specifying each address. Turning on the REPEAT switch causes timing pulse SP4 to trigger a one-shot which produces a delay, the length of which is adjustable by means of the coarse and fine SPEED controls on the operator console. When the one-shot reverts to its stable state, the level transition appearing at the output terminal is applied to the special pulse generator and initiates time state SP0 once more. The CP then repeats the operation associated with the manual key that is pressed.

3.2.3.7 READ-IN Key - The READ-IN key permits information punched in binary format on paper tape to be loaded into memory at successive memory locations, starting at the address specified by the ADDRESS switches. When in the binary mode, tape holes 1 through 6 of each line of tape contain one-third of an 18-bit word; hole 7 is not punched until the last line of the last character that is to be read, and hole 8 is always punched to cause the line to be read. When the READ-IN key is pressed, the processor selects the reader in binary mode, then waits for the reader to read three lines of tape and assemble these in the reader buffer in the form of an 18-bit word (and also waits until the READ-IN key is released). When the reader buffer is full, its contents are transferred to the AC and then deposited

in memory. The process of reading three lines of tape, assembling the information into an 18-bit word, and depositing words at consecutive memory locations continues until the reader encounters a line of tape in which hole 7 is punched. The reader then stops, and the processor executes the last 18-bit word read and deposited (hole 7 being in the last line of this word).

Pressing the READ-IN key causes the RUN flip-flop to be cleared at time SP0 and the MA to be cleared at time SP1. The following takes place:

a. At time SP1, a BGN pulse clears the special mode flip-flops, including the RPT (read paper tape) flip-flop to establish initial conditions. The PC is cleared, and the major state generator is forced to the execute state.

b. At time SP2, the address specified by the ADDRESS switches is set into the PC, and the operation code for DAC is set into the IR.

c. At time SP3, the RPT flip-flop is set to 1.

d. At time SP4, the AC is cleared and the contents of the PC are transferred to the MB. At this time a command is generated that selects the reader in binary mode and causes it to read three lines of tape successively into the reader buffer. When the reader buffer is full, the reader flag is set to 1.

e. The processor now waits for three conditions to be met:

(1) The RPT flip-flop is in the 1 state (this condition was fulfilled at time SP3).

(2) The reader flag is set to 1 (indicating that the reader buffer is full).

(3) The READ-IN key is released. If the processor is not forced to wait for this condition to be fulfilled, the rapid action of the reader may cause several words to be deposited at the starting address, with consequent loss or invalidation of information.

The levels representing assertion of these three conditions are combined in a gate; whichever of the three conditions is fulfilled last causes a level transition to occur at the output of the gate. This transition starts the main timing chain and initiates a computer cycle in the execute state.

f. The events in the execute cycle follow the pattern already described for a deposit operation. However, the CP does not stop at time T7 because timing pulse TP7, combined with the 1 state of the RPT flip-flop, causes the generation of timing pulse SP0 of a second readin operation. However, the RUN flip-flop is cleared at time SP0.

g. At time SP1 of a second (or subsequent) readin operation, no BGN pulse is generated, because the READ-IN key has been released. Further, since the RPT flip-flop remains set,

the PC is not cleared at time SP1 and the contents of the ADDRESS switches are not transferred to the PC at time SP2. Instead, the contents of the PC are incremented by 1 at time SP2. Thus, 18-bit words transferred from the reader buffer to the AC are deposited at consecutive memory locations.

h. When the reader encounters a line of tape which has hole 7 punched, the assertion level produced by hole 7 causes the RPT flip-flop to be cleared and the RUN flip-flop to be set at time T5.

i. At time T7, since the computer is in the execute state and the RUN flip-flop is set, timing pulse TP7 forces the major state generator to the fetch state and restarts the main timing chain. At time T1 of the ensuing fetch cycle, the contents of the PC are transferred to the MA. Therefore, since at that time the PC contained the memory address of the last word read from paper tape, the processor executes that word. The word may be any instruction, but sensible choices for the programmer would be either a HLT (halt) instruction allowing manual control of the program before starting or a JMP (jump) instruction providing entry to the start of the program.

3.2.3.8 SINGLE INSTRUCTION Switch - The SINGLE INSTRUCTION switch, in combination with an F SET level ("instruction done" situation), generates a RUN STOP signal that resets the RUN flip-flop and halts the CP at the end of the current memory cycle. However, the F SET ("instruction done") level is generated only during the cycle that completes the execution of an instruction and does not appear during a fetch or defer cycle which must be followed by an execute cycle. Thus, when the SINGLE INSTRUCTION switch is turned on, the CP halts after completing each instruction; and the next instruction must be initiated by pressing the CONTINUE key. When the SINGLE STEP and SINGLE INSTRUCTION switches are both turned on, the SINGLE STEP switch takes precedence; and the CP halts after each memory cycle.

3.2.4 Programmed Operations

The normal mode of PDP-7 operation is the execution of programmed instructions. A program interrupt (produced by peripheral equipment to transfer control of the CP from the main program to a subroutine),can modify programmed operation. A data break or a clock break can also temporarily interrupt the main program. During a data break, lasting one memory cycle, a high-speed peripheral device, which has a 15-bit address register as well as an 18-bit data register, can transfer information to or from memory. During a clock break, also lasting one memory cycle, a real-time clock may add 1 to the contents of memory location 7. If an overflow occurs, a program break is initiated; otherwise the main program is resumed.

When a program is to be executed, the starting address of the program is preset on the ADDRESS switches, and the START key is momentarily pressed. The CP fetches the first instruction from the specified address and executes it, at the same time adding 1 to the contents of the PC. Succeeding instructions are obtained from numerically consecutive memory locations, unless a JMP or JMS instruction changes the contents of the PC so that instructions are obtained from another block of numerically consecutive locations in a different section of memory.

Programming is simplified and memory space is conserved if the programmer arranges the instructions for an operation performed many times during the course of the program in the form of a subroutine. A subroutine is a group of instructions contained in a numerically consecutive block of memory locations that do not form part of the main program sequence. These subroutines may be entered from any part of the main program by means of a JMS (jump to subroutine) instruction which stores in memory the location of the next main program instruction (that is, the contents of the PC). The next instruction to be executed is the first instruction of the subroutine. Exit from the subroutine and return to the main program sequence is obtained by means of a JMP I (jump indirect) instruction, which directs the CP to the location containing the next main program instruction and effects the execution of the instruction found in that location.

The instructions performed by the PDP-7 are of two kinds: memory reference instructions and augmented instructions. A memory reference instruction contains an operation code in bits 0 through 3, and the location in memory of the word upon which the operation is to be performed in bits 5 through 17. If bit 4 is a 1, it is an indication that the address contained in the instruction word is not that of the operand itself, but is the location containing the address of the operand. This facility is known as indirect addressing. Indirect addressing has many uses; for example, it may be used with a jump instruction to permit reentry into the main program from a subroutine; it permits a memory location outside the current 8K field to be addressed when the extend mode is enabled; and it permits a programmer to gain access to an operand whose absolute address is determined by the program itself but known to be contained in a specific memory location.

An augmented instruction requires no reference to memory. An operation code in bits 0 through 3 identifies the instruction as an OPR/LAW, IOT, or EAE instruction. The contents of the remaining bits specify operations which timing pulses T5, T6, and T7 perform during a single computer cycle. More than one such microinstruction may be combined into a single instruction provided that there is no logical conflict between the operations specified.

The following paragraphs first describe the memory reference instructions and then the augmented instructions. The load accumulator (LAC) and operate (OPR) instructions are described in detail, as representative of the memory reference instructions and augmented instructions, respectively. Remarks on the remaining instructions are confined to important points not obvious from the flow diagram. All of the explanations assume that direct addressing is employed (bit 3 contains a 0). An explanation of the

use of the autoindexing locations and of the use of a defer cycle to permit indirect addressing follows the descriptions of the memory reference instructions. The descriptions of both memory reference and augmented instructions also assume that no I/O device has requested a break of any kind. The conditions under which a break may be granted and the events during the ensuing break cycle are described after the explanation of the augmented instructions.

3.2.4.1 Memory Reference Instructions

TABLE 3-1 MEMORY REFERENCE INSTRUCTIONS

Mnemonic Symbol	Octal Code	Machine Cycles	Operation Executed
CAL	00	2	Call subroutine. The address portion of this instruction is ignored. The action is identical to JMS 20.
DAC Y	04	2	Deposit AC. The contents of the AC are deposited in the memory cell at location Y.
JMS Y	10	2	Jump to subroutine. The contents of the PC and the contents of the L are deposited in memory cell Y. The next instruction is taken from cell Y + 1.
DZM Y	14	2	Deposit zero in memory cell Y.
LAC Y	20	2	Load AC. The contents of Y are loaded into the AC.
XOR Y	24	2	Exclusive OR. The exclusive OR is performed between the contents of Y and the contents of the AC, with the result left in the AC.
ADD Y	30	2	Add (1s complement). The contents of Y are added to the contents of the AC in 1s complement arithmetic and the result is left in the AC.
TAD Y	34	2	1s complement add. The contents of Y are added to the contents of the AC in 2s complement arithmetic and the result is left in the AC.
XCT Y	40	1+	Execute. The instruction in memory cell Y is executed.
ISZ Y	44	2	Increment and skip if zero. The contents of Y are incremented by one in 2s complement arithmetic. If the result is zero, the next instruction is skipped.
AND Y	50	2	AND. The logical operation AND is performed between the contents of Y and the contents of the AC with the result left in the AC.

TABLE 3-1 MEMORY REFERENCE INSTRUCTIONS (continued)

Mnemonic Symbol	Octal Code	Machine Cycles	Operation Executed
SAD Y	54	2	Skip if AC is different from Y. The contents of Y are compared with the contents of the AC. If the numbers are different, the next instruction is skipped.
JMP Y	60	1	Jump to Y. The next instruction to be executed is taken from memory cell Y.

a. Load Accumulator (LAC)

The LAC instruction is a memory reference instruction which requires a fetch and and execute cycle. During the fetch cycle, the address of the LAC instruction is transferred from the PC to the MA, and the contents of the PC are incremented by 1. A read operation transfers the contents of the memory cell addressed into the MB, and bits 0 through 3 are transferred directly into the IR as the operation code of the instruction to be executed. The contents of the MB are then rewritten into the memory cell from which they were read. Finally, the major state generator is set to the execute state. During the execute cycle, the operand is extracted from memory and loaded into the accumulator. The following detailed description of the sequence is read while referring to the flow diagram and to the specified engineering logic diagrams.

At time T1 of any fetch cycle, the instruction register must be cleared. The F level is NAND combined with the T1 pulse (D5,7); and the gate output, after amplification and inversion, is applied to the direct clear inputs of the four IR flip-flops. (In a similar manner, the IR is cleared at time T1 of a break cycle and at time T2 of certain execute cycles. The IR is not cleared during a defer cycle.) Also at time T1, the F negative level is NAND combined with the T1 pulse (C7, 8) to produce a PC1 →MA pulse. This pulse is applied to a set of MA input gates, opening those already conditioned by a negative level from a PC flip-flop in the 1 state.

Note that the PC1 →MA pulse is applied only to bits 5 through 17 of the MA register. Bits 3 and 4 of this register are used only in conjunction with memories of 16K capacity or more and must receive a separate transfer pulse (EPC1 →EMA) from the memory extension control unit. The F level and T1 pulse are also NAND combined in the PC control logic (E6, 8) to produce a +1 →PC pulse which increments the contents of the PC by 1. The +1 →PC pulse complements bit 17 of the PC register (F8, 15), and is also applied to a gated pulse amplifier. If this gate is already conditioned by a PC17 (1) level, a carry pulse

complements bit 16. A series of gated pulse amplifiers propagates the carry toward bit 5 and stops when it first encounters a bit in the 0 state. The flip-flops have a controlled internal delay so timed that the MA input gates open and close before the incrementing pulse causes any flip-flop to change state. It is this internal delay which permits the PC register to be sampled and incremented by simultaneous pulses without transferring the incremented, rather than the original, contents to the MA.

At time T2 of every computer cycle, the MB is cleared and a read operation is prepared. Time pulse T2 is applied to an isolating gate (D3, 8), and the output of the gate causes a pulse amplifier to produce the 0 → PC pulse. The TP2 pulse sets the READ flip-flops of the memory control (27) to 1 and is NAND combined with the MA4 (0) level to produce the TP2 · SEL 0, 1 pulse (C8, 10). Note that the MA4 bit is always 0 unless more than 8K of memory capacity is in use. The memory control decodes the MA5 bit to produce either a SEL 0 or a SEL 1 level used to select one of the two 4K memory stacks in the standard 8K field. The SEL level is combined with the 1 output of the READ flip-flops to produce an appropriate SEL · READ LEVEL, which is applied to memory. Paragraph 3.4 discusses in detail the action of the memory. The effect of the SEL and SEL · READ levels is to enable the half-select X and Y read circuits in memory. The TP2 · SEL 0, 1 pulse applied to a delay network in memory produces a strobe pulse which goes to the sense amplifiers of the memory. This strobe pulse clears the READ 2 flip-flop and returns to the main timing chain as the STB RTN pulse, which initiates the generation of T3 and clears the READ 1 flip-flop.

When the strobe pulse occurs, the memory sense amplifiers compare the signal level in the sense winding of each core plane with a reference level. In planes where coincident read currents have caused a core in the 1 state to change to the 0 state, the sense signal is greater than the reference level; and the associated sense amplifiers (SA) produce standard negative pulses. These SA pulses are applied to the MB input gates and set the corresponding MB flip-flops. An $\overline{\text{MB STB INH}}$ negative level generated in the MB control normally enables the SA → MB input gates. Thus, the contents of the addressed memory cell are transferred to the MB unless the control logic specifically inhibits the gates. During a fetch cycle, when the MB is loaded with an instruction word consisting of an operation code and the address of the operand, the four most significant bits (which contain the operation code) are transferred directly into the IR, as well as into the MB. The negative pulses from sense amplifiers SA0 through SA3 are applied to IR input gates conditioned by the fetch level (D7, 7), and set the IR flip-flops accordingly.

After the strobe pulse has occurred, the contents of the various registers are as follows:

ADDRESS switches	Z (address of the first instruction, which in this example is LAC Y)
PC	Z+1
MA	Z
MB	MB0 through MB3 contain octal 20 (=LAC)
	MB4(0) (= no indirect address)
	MB6 through MB17 contain Y (address of operand)
IR	IR0 through IR3 contain octal 20 (=LAC)

In the instruction register, the states of IR0(0) and IR1(1) are decoded to produce an IA1 level and an $\overline{IA3}$ level. The states of IR2(0) and IR3(0) are decoded to produce IB0 level. The $\overline{IA3}$ level, which identifies the instruction as a memory reference instruction, is NAND combined with the existing fetch (F) and MB4(0) levels (E1, 7) to establish a SET level. This ground level conditions the DCD gate (D3, 7) associated with a pulse amplifier which sets an execute (E) state into the major state generator at time T7. At the same time the ground level disables input L of module L21 to prevent any break request from being granted until the execution of the instruction.

At time T4, timing pulse TP4 sets the INH flip-flop of the memory control logic, thus enabling the inhibit supply of the memory. At time T5, both WRITE flip-flops are also set and, in conjunction with the SEL 0 level, established coincident writing currents through the cores of memory cell Z. All cores of the addressed cell are driven by full-select write currents. However, those in planes which correspond to MB bits containing a 0 are inhibited from changing state by a half-select inhibit current in the read direction. Thus, the contents of the MB are written back into the cell from which they are read.

At time T6, timing pulse TP6 resets the WRITE 1, WRITE 2, and INH flip-flops, and the writing operation is now complete. At time T7, timing pulse TP7 INVTD is applied to the DCD gates of the major state generator (24) and, in combination with the E SET level established during T3, sets the execute (E) state. The RUN flip-flop is still set, and the RUN (1) level is NAND combined with timing pulse T7 (C8, 8) to produce a 0 $\rightarrow$MA pulse which clears all the flip-flops of the MA. The RUN(1) level is also combined with a $\overline{SLOW\ CYC}$ (not slow cycle) level to condition a DCD gate at the entry to the main timing chain (F1,5). The TP7 pulse (delayed 150 nsec) is combined with a $\overline{STOP\ CP\ TC}$ (not stop central processor timing chain) level signifying that the extended arithmetic element does not require an

interruption. The resulting pulse triggers the DCD gate and energizes a pulse amplifier (F2, 5). The output of this pulse amplifier causes the generation of timing pulse TP1, thereby initiating the second (execute) computer cycle.

At time T1 of the execute cycle, the absence of an IA0 signal at terminal S of module F5 (C1, 8) results in the production of a $\overline{\text{CAL}}$ (not CAL instruction) level. This level is NAND combined in the MA control (C7, 8) with the T1 timing pulse and another negative level resulting from the absence of a defer (D) level. The output of the NAND gate is applied to a pulse amplifier which produces an MB1 → MA pulse. This pulse opens all MA input gates already conditioned by a negative level from an MB flip-flop in the 1 state; thus the address of cell Y (containing the operand) is set into bits 5 through 17 of the MA. The (E) level of the major state generator is NAND combined with the IA1 level produced by the IR, and the output of the gate is inverted to produce an E · IA1 level (F2, 9). The E · IA1 level is NAND combined with the IB0 level and inverted to produce an E · LAC level. The E · LAC level enables a NAND gate which is opened by time pulse T1 to trigger a pulse amplifier in the AC control logic (C6, 9). This pulse amplifier produces a 0 → AC pulse which clears all the flip-flops of the accumulator.

During the execute cycle, the contents of memory cell Y are read into the MB and then rewritten into memory in exactly the same manner as for cell Z (during the fetch cycle). Therefore, the following paragraphs describe only those events peculiar to the execute cycle. After the strobe occurs, the contents of the various registers are as follows:

PC	Z+1
MA	Y
MB	Contents of cell Y
IR	Octal 20 (= LAC)
AC	All 0's

At time T3 of the execute cycle, the E · IA1 level is combined with the T3 timing pulse. The resulting pulse is applied to pulse amplifier PA2 of module J2 in the AC control logic, and the output of the pulse amplifier is an XOR → AC pulse. This pulse is applied to a set of accumulator register input gates normally used to complement the accumulator in an exclusive OR operation. However, since the accumulator is cleared at time T1 (of the execute cycle), no carry pulses can be generated; and the effect is a simple transfer of memory buffer 1's into the corresponding bits of the accumulator.

After the operand has been rewritten into memory cell Y (starting at time T4) the MA is cleared, and the interrupt control is interrogated to determine the state to be set into the major state generator for the next cycle. If any I/O device has initiated a break

request, the interrupt control logic (14) establishes a negative BK RQ (break request) level which is applied to terminal K of module K20 in the major state generator. Then, provided that neither a D SET nor an E SET level has previously been established by the nature of the instruction, a B SET ground level appears at terminal N of the module. This level, in combination with timing pulse TP7 INVTD, sets the major state generator to the break (B) state for servicing the I/O device. If there is no break request, the $\overline{\text{BK RQ}}$ combines with $\overline{\text{D SET}}$ and $\overline{\text{E SET}}$ levels to produce an F SET level; and, at time T7, a new fetch cycle is initiated to extract the next instruction from memory address Z+1. Note that a break request is never granted until the current instruction has been executed. Thus, a break can be granted only after completion of a 1-cycle instruction, after the execute cycle of a multicycle instruction, or after a break cycle to continue a block transfer or other operation involving several break cycles.

b. Exclusive OR (XOR)

The exclusive OR logical operation is performed between the contents of the AC and the contents of the MB and requires a fetch cycle and an execute cycle. During a fetch cycle, the operation code 24 is set into the IR; and the address of the operand is set into bits 5 through 17 of the MB. At time T1 of the execute cycle, the address of the operand is transferred from the MB to the MA. At time T2, the MB is cleared; and a read operation sets the operand into bits 0 through 17 of the MB. The E negative level of the major state generator is NAND combined in the AC control with the IA1 negative level produced by the IR decoder. The resulting E · IA1 negative level is combined in the AC control with timing pulse T3 to produce a negative XOR →AC pulse. This pulse opens AC input gates already conditioned by MB bits in the 1 state and complements the associated AC bits. When the AC has previously been cleared (as in the LAC instruction), the XOR→ AC command can be used for a simple transfer of binary 1s from MB to AC.

c. 1s Complement Add (ADD)

The ADD instruction adds the contents of the MB to the contents of the AC in 1s complement arithmetic and requires a fetch cycle and an execute cycle. During the fetch cycle, the operation code 30 is set into the IR; and the address of the operand is set into bits 5 through 17 of the MB. At time T1 of the execute cycle, the address of the operand is transferred from the MB to the MA. At time T2, the MB is cleared, and a read operation sets the operand into bits 0 through 17 of the MB. At time T3, the E · IA1 negative level causes an XOR operation to be performed in the manner already described. In

the AC control, the E negative level is further combined with the IB2 level produced by the IR decoder to produce an E · ADD level. The E · ADD level, in combination with timing pulse T4, produces a negative AC CRY (accumulator carry) pulse. This carry pulse opens accumulator input gates in which the state of each AC bit is compared with the state of the corresponding MB bit and carries are propagated where necessary. A carry pulse generated by bit AC0 causes the generation of a negative END CRY (end carry) pulse. The END CRY pulse is applied to the complementing input of the AC17 flip-flop; if this is already in the 1 state, further carries are propagated toward bit AC0.

d. 2s Complement Add (TAD)

The TAD instruction adds the contents of the MB to the contents of the AC in 2s complement arithmetic and requires a fetch cycle and an execute cycle. During the fetch cycle, the operation code 34 is set into the IR; and the address of the operand is set into bits 5 through 17 of the MB. At time T1 of the execute cycle, the address of the operand is transferred from the MB to the MA. At time T2 the MB is cleared, and a read operation sets the operand into bits 0 through 17 of the MB. At times T3 and T4, XOR and carry operations are performed as described for the ADD instruction. At time T5 an overflow from bit AC0 causes generation of a TAD CRY (2s complement carry) pulse which sets the link flip-flop to 1. The effect of the link depends upon what instruction follows; for example, it may be sensed by an augmented instruction to cause a skip.

e. Execute (XCT)

The XCT instruction causes the CP to execute the instruction contained in the memory cell addressed. The instruction requires a fetch cycle plus the cycles required to perform the instruction contained in the cell. During the fetch cycle of an SCT instruction, the operation code is set into the IR; and the address of the instruction to be performed is set into bits 5 through 17 of the MB. At time T1 of the execute cycle, the address of the instruction is transferred from the MB to the MA. At time T2, the IR is cleared, and a fetch state is forced. Between times T2 and T3, the contents of the addressed memory cell are read into the MB; and the four most significant bits (containing the operation code) are set into the IR. The CP then executes the instruction contained in the cell addressed by the XCT instruction. Note that even if the subject instruction is a memory reference instruction, the effective address of the operand is available without

reference to the PC, so that the program sequence is unaltered. In other words, the CP seems to be performing the subject instruction in place of the SCT instruction, then proceeds to the instruction following the XCT instruction.

f. Index and Skip if Zero (ISZ)

The ISZ instruction increments the contents of the addressed cell by 1, using 2s complement arithmetic. If the incremented number is 0, the next instruction is skipped. The ISZ instruction requires a fetch cycle and an execute cycle. During the fetch cycle, the operation code 44 is set into the IR; and the address of the operand is set into bits 5 through 17 of the MB. At time T1 of the execute cycle, the address of the operand is transferred from the MB to the MA. Between times T2 and T3, a read operation sets the operand into the MB. The E level derived from the major state generator is combined in the MB control with the IA2 and IB1 levels produced by the IR decoder. The resulting E · ISZ level conditions a gate which is opened by timing pulse TP3 to produce a +1 →MB negative pulse. This pulse complements the least significant bit of the MB and is also applied to the MB gates which propagate carry pulses. If the MB overflows (which can only happen when the contents of the MB become 0), bit MB0 generates a carry pulse which is combined in the PC control with the E · ISZ level. As a result, a negative pulse is generated which increments the contents of the PC by 1. Starting at time T4, the incremented contents of the MB are written back into the memory cell addressed by the ISZ instruction. Note that at time T1 of the fetch cycle the address of the ISZ instruction is set into the MA; and the contents of the PC are incremented in the normal manner. If the incremented contents of the MB are not 0 and therefore produce no overflow at time T3 of the execute cycle, the next instruction is fetched and executed. An overflow from the MB, however, causes the contents of the PC to be incremented again, so that the instruction immediately following ISZ in the program is skipped.

g. Logical AND (AND)

The logical AND operation is performed by a transfer of 0s from the MB to the AC. Thus, at the end of the operation, all bits of the AC have been cleared except those bits containing a 1 both in the AC and in the operand before the operation started. The AND instruction requires a fetch cycle and an execute cycle. During the fetch cycle, operation code 50 is set into the IR; and the address of the operand is set into bits 5 through 17 of the MB. During the execute cycle, the address of the operand is transferred from the MB to the MA at time T1. Between times T2 and T3, the operand is read into the MB. The E level derived from the major state generator is combined in the AC control with the IA2 and IB2 levels from

the IR decoder to produce an E · AND level. This level conditions a NAND gate, which at time T5 is triggered to produce an MB0→ AC pulse. The MB0 → AC pulse clears all AC bits corresponding to MB bits which are in the 0 state. AC bits which are already in the 0 state remain 0s, regardless of the state of the corresponding MB bit. AC bits which are in the 1 state remain 1s only if they correspond to MB bits in the 1 state.

h. Skip if AC is Different from Operand (SAD)

The SAD instruction sets the operand into the MB and performs an XOR operation between the MB and the AC. No carry pulses are propagated, so that if the initial contents of the AC are identical to that of the MB, the end contents of the AC will be 0, and the next instruction will be performed. If any bit of the AC differs from the corresponding bit in the MB, the next instruction is skipped.

The SAD instruction requires a fetch cycle and an execute cycle. During the fetch cycle, the operation code 54 is set into the IR and the address of the operand is set into bits 5 through 17 of the MB. The contents of the PC are incremented in the normal manner. At time T1 of the execute cycle, the address of the operand is transferred from the MB into the MA and a read operation sets the operand itself into the MB.

The E level derived from the major state generator is combined in the AC control with the IA2 and IB3 levels from the IR decoder to produce an E · SAD level. The E · SAD level conditions a gate which is opened at time T3 to produce a negative XOR pulse. The XOR pulse causes MB bits in the 1 state to complement the corresponding bits of the AC. No carry pulses are propagated, so that if the initial contents of the AC are identical to that of the MB, the resultant contents of the AC are all 0s. A 17-input AND gate in the AC control samples the status of all the AC flip-flops at time T5 and generates an AC=0 level only if all flip-flops are in the 0 state. The AC=0 level is combined in the PC control with the E · SAD level to generate a +1→ PC pulse which increments the contents of the PC by 1. Thus, if the initial contents of the AC are identical to that of the operand, the next instruction is skipped. If any one AC flip-flop is in the 1 state after the XOR operation (indicating that the contents of the AC are different from that of the operand), the AC=0 level is not produced by the AC control gate, and the +1 → PC pulse is not generated. The CP, therefore, proceeds to the next instruction and executes it. The XOR operation is repeated at time T6 to restore the original contents of the AC.

i. Deposit AC in Memory (DAC)

The DAC instruction deposits the contents of the AC in memory at the address specified in the instruction. The instruction requires a fetch cycle and an execute cycle. During the fetch cycle, the operation code 04 is set into the IR, and the address where the contents of the AC are to be deposited is set into bits 5 through 17 of the MB. At time T1 of the execute cycle, the address for the deposit is transferred from the MB to the MA. The E level derived from the major state generator is combined in the MB control with the IA0 and IB1 levels from the IR decoder to produce an E · DAC level. This causes an AC1 → MB pulse to be generated at time T3. The AC1 → MB pulse opens the gates connecting the output of the AC to the input of the MB. A write operation (starting at time T4) deposits the new contents of the MB into memory at the address specified by the DAC instruction. Note that although read currents are applied to the addressed cell, the combination of the E and IA0 levels in the MB control produces an MB STB INH (MB strobe inhibit) level that inhibits the gates between the sense amplifiers and the input of the MB. Therefore, the original contents of the addressed cell are not transferred into the MB, and are lost. Note also that when a pseudo-DAC instruction is used for loading information from perforated tape, the RPT(1) level causes the generation of a SEL → RRB pulse at time T2, which transfers the contents of the reader buffer into the AC. For further details, refer to the description of the READ-IN key in section 3.2.3. At the end of a readin operation, the combination of the RPT(1) level and a reader hole 7 signal clears the RPT flip-flop and sets the RUN flip-flop at time T5. The fetch state is then established for the execution of the next instruction. However, if the readin operation is to continue, the RPT(1) level causes the MB to be cleared at time T7 and starts the special pulse generator.

j. Deposit Zero in Memory (DZM)

The DZM instruction clears the memory cell at the address specified in the instruction and requires a fetch and an execute cycle. During the fetch cycle, the operation code 14 is set into the IR; and the address for the deposit is set into bits 5 through 17 of the MB. At time T1 of the execute cycle, the address for the deposit is transferred from the MB to the MA. At time T2, the MB is cleared, and a read operation is initiated in the normal manner. The E level derived from the major state generator is combined in the MB control with the IA0 level from the IR decoder, thereby inhibiting the gates between the memory sense amplifiers and the MB. Information previously stored in the addressed cell is read, but does not reach

the MB and is lost. A normal write operation takes place, starting at time T4; but since the MB is cleared, 0 is written into the addressed cell. At the end of the execute cycle, the fetch state is established in preparation for execution of the next instruction.

k. Jump to Subroutine (JMS)

The JMS instruction permits exit from the main program into a subroutine and requires a fetch and an execute cycle. During the fetch cycle, the operation code 10 is set into the IR; and an address (Y) is set into bits 5 through 17 of the MB. At time T1 of the execute cycle, address Y is transferred from the MB into the MA. At time T2, the MB is cleared and the input gates are inhibited; so that the normal read operation destroys the original contents of cell Y. At time T3, the current program count and the status of the link are transferred to the MB; the PC is then cleared. This information is written into cell Y and is available there when reentry into the main program is desired. At time T4, the address Y is transferred from the MA to the PC; and at time T5, the contents of the PC are incremented by 1. The end contents of the PC are Y+1, the address from which the first instruction of the subroutine is fetched.

l. Call Subroutine (CAL)

The CAL instruction is equivalent to the instruction JMS 20. During the fetch cycle, the operation code 00 is set into the IR; and the IR decoder produces IA0 and IB0 levels. These are combined in the MB control with a $\overline{B}$ (not a break state) level to produce a CAL level. At time T1 of the execute cycle, the CAL level is combined in the MA control with the E level derived from the major state generator and generates a 20→ MA pulse. This pulse sets octal 20 into the MA by setting flip-flop MA 13 to the 1 state. The 20 → MA pulse also sets flip-flop IR2, thereby setting operation code 10(JMS) into the IR. Thereafter, the CP proceeds to execute the JMS instruction, depositing the link status and current program count at memory location 20 and taking the first instruction of the subroutine from memory location 21, as described in the explanation of the JMS instruction.

m. Jump (JMP)

The JMP instruction transfers control of the CP to a sequence of consecutive memory locations that begin at the address specified in the instruction. The JMP instruction requires only one cycle (fetch), during which the operation code 60 is set into the IR; and the memory location from which the next instruction is to be taken is set into bits 5 through 17 of the MB. The IA3 and IB0 levels derived from the IR decoder are combined in the major state logic to produce a JMP level which conditions two gates in the PC control. At time T5, one of these

gates is triggered to produce a 0 → PC pulse which clears the PC. At time T6, the second gate is triggered to produce an MB1→ PC pulse which transfers the address specified by the JMP instruction into the PC. The major state generator is then set to fetch, and, during the following cycle, the next instruction is fetched from that address.

n. Indirect Addressing and Autoindexing

When bit 4 of a memory reference instruction contains a 1, the CP interprets the contents of bits 5 through 17 as the memory location where the address of the operand may be found. At time T7 of the fetch cycle, the major state generator is set to defer instead of to execute. At time T1 of the defer cycle, the contents of the MB are transferred to the MA (unless the instruction is CAL). The MB is then cleared, and a read operation sets the contents of the addressed cell into the MB, which now holds the effective address of the operand. If this address is one of the eight autoindexing locations 10_8 through 17_8, decoding gates in the MA generate a pulse which increments the contents of the MB by 1 at time T3. If the instruction containing the indirect address was a JMP instruction, the PC is cleared at time T5; the effective address of the next instruction is transferred from MB to PC at time T6; and the major state generator is set to fetch at time T7. If the instruction was not a JMP, no action occurs at times T4 through T6. The major state generator is set to execute at time T7. At time T1 of the execute cycle, the effective address of the operand is transferred from MB to PC. The machine then performs the operation specified by the instruction upon the operand contained in the indirectly addressed cell.

The eight auto-index locations may contain either the effective address of an operand or an instruction, depending on the program requirements. When used as direct addresses, they are identical to other memory locations. When used as indirect addresses, however, their contents are incremented by 1 each time they are addressed. Thus, use of the autoindexing locations facilitates the repetition of an arithmetic process on a series of numbers without performing separate arithmetic operations on the addresses concerned. The PDP-7 User Handbook explains the uses of the autoindex locations from the programmer's viewpoint.

3.2.4.2 Augmented Instructions - The augmented instructions are of three groups: EAE instructions with the OP code 64, which are discussed in chapter 4; IOT instructions with the OP code 70 which are discussed in the PDP-7 Interface and Installation Manual, F78A; and the OPR instructions with the OP code 74. All three augmented instruction groups can be microprogrammed to perform several non-conflicting operations in a single instruction. See table 3-2 for the OPR instructions.

TABLE 3-2 OPR INSTRUCTIONS

Mnemonic Symbol	Octal Code	Event Time	Operation Executed
OPR or NOP	740000	---	Operate group or no operation. Causes a 1-cycle program delay.
CMA	740001	3	Complement accumulator. Each bit of the AC is complemented.
CML	740002	3	Complement link.
OAS	740004	3	Inclusive OR ACCUMULATOR switches. The word set into the ACCUMULATOR switches is OR combined with the contents of the AC; the result remains in the AC.
RAL	740010	3	Rotate accumulator left. The contents of the AC and L are rotated one position to the left.
RLR	740020	2	Rotate accumulator right. The contents of the AC and L are rotated one position to the right.
HLT	740040	---	Halt. The program is stopped at the conclusion of the cycle.
SMA	740100	1	Skip on minus accumulator. If the contents of the AC are negative (2s complement), the next instruction is skipped.
SZA	740200	1	Skip on zero accumulator. If the contents of the AC equal zero (2s complement), the next instruction is skipped.
SNL	740400	1	Skip on non-zero link. If the L contains a 1, the next instruction is skipped.
SKP	741000	1	Skip. The next instruction is unconditionally skipped.
SPA	741100	1	Skip on positive accumulator. If the contents of the AC are zero (2s complement) or a positive number, the next instruction is skipped.
SNA	741200	1	Skip on non-zero accumulator. If the contents of the AC are not zero (2s complement), the next instruction is skipped.
SZL	741400	1	Skip on zero link. If the L contains a 0, the next instruction is skipped.
RTL	742010	2,3	Rotate two left. The contents of the AC and the L are rotated two positions to the left.

TABLE 3-2 OPR INSTRUCTIONS (continued)

Mnemonic Symbol	Octal Code	Event Time	Operation Executed
RTR	742020	2,3	Rotate two right. The contents of the AC and the L are rotated two positions to the right.
CLL	744000	2	Clear link. The L is cleared.
STL	744002	2,3	Set link. The L is set to 1.
RCL	744010	2,3	Clear link, then rotate left. The L is cleared; then the L and AC are rotated one position left.
RCR	744020	2,3	Clear link, then rotate right. The L is cleared; then the L and AC are rotated one position right.
CLA	750000	2	Clear accumulator. Each bit of the AC is cleared.
CLC	750001	2,3	Clear and complement accumulator. Each bit of the AC is set to contain a 1.
LAS	750004	2,3	Load accumulator from switches. The word set into the ACCUMULATOR switches is loaded into the AC.
GLK	750010	2,3	Get link. The contents of L are set into AC17.
LAW N	76XXXX	---	Load the AC with LAW N.

a. Operate (OPR)

The bit assignment of an OPR instruction is shown in figure 3-1. It is seen that bit 5 is used in one instruction only, i.e., clear accumulator (CLA) for which the octal code is 750000. All other instructions of the OPR class have octal codes beginning with 74. The functions performed at times T1 through T4 of an operate instruction are exactly the same for those which occur in the fetch cycle of any other kind of instruction. The IA3 and IB3 levels from the IR decoder are combined in the AC control with the MB4(0) level to produce the OPR level. This level conditions two gates: one is triggered at time T5 to perform one set of operations and the other gate is triggered at time T7 to perform the second set of operations. The first set of commands consists of the following:

(1) If bit 5 is a 1, the AC is cleared.

(2) If bit 6 is a 1, the link is cleared.

(3) If bits 7 and 13 are 1s, the AC is rotated one place right (and will be rotated again during time T7).

(4) If bits 7 and 14 are 1s, the AC is rotated one place left (and will be rotated again during time T7).

(5) If bit 12 is a 1, the RUN flip-flop is cleared and the program is halted at the conclusion of the current memory cycle.

(6) If bit 8 is a 0, any one of the following conditions increments the contents of the PC to skip the next instruction: link is not 0 (bit 9 is a 1); AC is not 0 (bit 10 is a 1); AC is negative (bit 11 is a 1).

The second set consists of the following operations which take place in time T7:

(1) If bit 13 is a 1, the AC is rotated one place right.

(2) If bit 14 is a 1, the AC is rotated one place left.

(3) If bit 15 is a 1, the contents of the accumulator switch register are inclusively OR combined with the contents of the AC.

(4) If bit 16 is a 1, the link is complemented.

(5) If bit 17 is a 1, the AC is complemented.

Note that because of the nature of the rotate operations, a rotate operation may not be combined with any other operation of the same set. For example, a single instruction may clear the link (first set) and rotate the AC one place (second set); but a 2-place rotation (both sets) precludes the instruction from performing any other operation.

b. Law (LAW)

The LAW instruction is a special case of an operate class instruction and has the operation code 76. The IR decoder produces IA3 and IB3 levels which are combined in the AC control with the MB4(1) level to produce an OP LAW level. This level conditions two AC control gates: one is triggered at time T5 to clear the AC and the other at time T6 to perform an XOR operation between MB and AC. This effectively places the entire instruction in the AC. Thus, an address-sized number (15 bits), preceded by the operation code, can be loaded into the AC without using an extra memory location. The various uses of the LAW instruction are described from the programmer's viewpoint in the PDP-7 User Handbook.

c. Input/Output Transfer (IOT)

IOT instructions are augmented instructions which can be microprogrammed to address an I/O device and to generate up to three time pulses to initiate and control the operation of the device. When an IOT instruction is executed, if bit 14 is a 1, the AC is cleared at time T5; if bit 17 is a 1, an IOP1 pulse is also generated at this time. If bit 16 is a 1, an IOP2 pulse is generated at time T7. If bit 15 is a 1, an IOP3 pulse is generated at time T1 of the following cycle.

3.2.4.3 Break Cycle - A break cycle provides a temporary interruption of the main program during which information may be transferred to or from a high-speed peripheral device or a subroutine may be initiated to service a slow peripheral device. Reference to the flow diagram (4) shows that a break cycle may be entered under the following conditions (which indicate an "instruction done" situation):

a. After the fetch cycle of an OPR, LAW, IOT, or directly addressed JMP instruction.

b. After the defer cycle of an indirectly addressed JMP instruction.

c. After the execute cycle of a directly or indirectly addressed memory reference instruction.

d. After a break cycle to continue a block transfer or other operation involving several break cycles.

When a break request from peripheral equipment is granted, one of three possible sequences takes place during the break cycle. If two or more break requests appear simultaneously, break sequences are granted in the following descending order of priority: data break, clock break, and program break.

a. Data Break

A data break may be granted to a high-speed I/O device containing registers which can simultaneously supply or accept a 15-bit address word, an 18-bit data word, a break request signal, and a direction-of-transfer signal. When a data break is granted, the IR is cleared; and the address specified by the I/O device is set into the MA at time T1 of the break cycle. If the I/O device specifies an outward transfer, the contents of the addressed memory cell are read into the MB between times T2 and T3 and are available there for sampling by the input register of the I/O device. If an inward transfer is specified, the gates between the sense amplifiers and the MB are inhibited. As a result, any information contained in the cell is destroyed, and the cell is cleared. At time T3 of the break cycle, the input gates linking the MB directly to the output register of the I/O device are triggered, and the incoming data is set into the MB.

A normal write operation, starting at time T4, writes the data into the memory cell. Use of the Type 173 Data Interrupt Multiplexer permits up to four high-speed I/O devices to share the data interrupt channel. (Refer to chapter 4 for further details.) After completion of the high-speed transfer, a fetch state is established for continuation of the program, unless a further break request exists. In this case, another break cycle follows.

b. Clock Break

A real-time clock, which can be enabled or disabled under program control by the appropriate IOT instruction, is included in each PDP-7 system. When the clock is enabled, each clock pulse initiates a break request. When the break is granted, the IR is cleared at time T1 of the break cycle. The clock address 7_8 is set into the MA and the clock count request flip-flop is cleared. Between times T2 and T3 the contents of memory location 7_8 (the clock count) are read into the MB and at time T3 the contents of the MB are incremented by 1, A normal write operation, starting at time T4, deposits the incremented clock count in memory location 7_8. If incrementing the MB does not cause an overflow, a fetch state is established at time T7 to continue the main program (unless there is a further break request). If incrementing the clock count causes the MB to overflow, a carry pulse is generated by bit MB0. This carry pulse sets the clock flag to 1, thereby initiating a program break. Possible programming uses of the real-time clock are described in the PDP-7 User Handbook.

Note that when the automatic priority interrupt (API) option is included in the PDP-7 system, the real-time clock is removed and the API is connected in its place. The real-time clock may then use one of the API channels. For further details of the API, refer to chapter 4.

c. Program Break

Slow I/O devices, such as the Teletype or paper tape reader, require an interval of several milliseconds between the time one information transfer is performed and the time when the device is ready for the next transfer. During this interval, the PDP-7 can perform many hundreds of programmed instructions. When programmed instructions enable one or more such devices, the program break facility permits the CP to continue execution of the main program until such time as a device indicates, by setting its flag, that it is ready to send or receive information. The setting of any device flag generates a program break request, and at the first "instruction done" situation the CP enters a break cycle in which the address of the next main program instruction, together with the status of the link, trap flag, and extend mode are stored at location 0. Control of the processor is then transferred to a subroutine starting in location 1, which scans all the device flags to discover which device caused the interrupt.

Identification of the interrupting device may provide entry to a further subroutine for servicing the device. At the conclusion of the servicing subroutine, the main program may be reentered by a jump indirect to location 0, which transfers program control to the address stored at location 0.

A program break is granted when all of the following conditions are fulfilled:

(1) The program interrupt facility is previously enabled by a programmed ION instruction.

(2) The setting of a device flag has generated a program break request.

(3) There is no data break in progress or waiting.

(4) There is no clock (or API) break in progress or waiting.

(5) There is no program break in progress.

At time T1 of the break cycle the IR is cleared, and at time T2 and MB is cleared. The memory generates read currents which clear location 0, but the MB input gates are inhibited so that any information previously contained in that location is destroyed. At time T3 the link status is set into bit MB0, the extend mode status into bit MB1, and the trap flag status bit into MB2. The contents of bits PC3 through PC17 are transferred to the corresponding bits of the MB and the PC is cleared. At time T4, the contents of the MA are transferred to the PC; note, however, that the MA is cleared at time T7 of the previous cycle and is not reloaded, so its contents are still 0. Also at time T4 a normal write operation is begun which deposits the contents of the MB in memory at location 0. At time T5, the contents of the PC are incremented by 1, so that the next instruction is taken from location 1 in which a subroutine starts. The program interrupt enable flip-flop is cleared to prevent any other program breaks until the interrupt is enabled by a programmed instruction at the conclusion of subroutine operations. Note, however, that data breaks and clock (or API) breaks may still be granted. If the program is operating in the trap mode and the program break is initiated by the trapping of an illegal instruction, the contents of the PC are again incremented by 1 at time T5. Thus, control of the CP is transferred to a subroutine starting in memory location 2 in order to identify the trapped instruction and take appropriate action. If no data break or clock break request is originated during the break cycle, a fetch state is established at time T7 and the first subroutine instruction is fetched during the ensuing fetch cycle. If a data or clock break request exists, a further break cycle is granted before the subroutine is entered.

3.2.4.4 Trap Mode - When the PDP-7 forms part of a real-time or multiuser system, the trap mode permits the use of sophisticated programming in the main program and guarantees this against interference from other users operating in a different section of memory. When the main program is operating in real time, it is particularly important to ensure that the processor cannot be halted, involved in lengthy operations, or thrown into a loop from which it cannot escape. The I/O trap provides the basic hardware necessary to provide protection against such disturbances.

When the trap mode is enabled by turning on the TRAP switch and by a programmed ITON (I/O trap on) instruction, the following illegal instructions are trapped: all IOT instructions, all HLT (halt) instructions, and all XCT (execute) instructions. When an illegal instruction is detected, the trap flag is set thereby preventing execution of the instruction. Instead, a program break request is initiated. When the break is granted, control of the CP is transferred to a subroutine starting at memory location 2, which initiates procedures for identifying the trapped instruction and for taking appropriate action. The reason for trapping IOT halt instructions is to prevent stopping the sequence at an undefined portion of the program. XCT instructions are trapped because if the subject instruction is also an XCT, a loop situation may arise in which the CP never encounters an "instruction done" situation, so that all control is lost.

3.3 PROCESSOR

This section describes in detail the logic elements which perform the logic functions described in 3.2. Descriptions of registers consider the effect of the various control signals applied; descriptions of control elements consider the output signals and explain the conditions under which each of these is generated. Many types of FLIP CHIP modules consist of a number of similar components (e.g., Type W607 contains three identical pulse amplifiers). Where necessary the individual components of a module are identified by their input and output terminal letters (e.g., NOR gate NPR of module J5). In addition, references to the zone of the engineering drawing in which the component is located aid in identification of a particular component.

All logic circuit elements of the processor appear on the block diagram of figure 3-2. These elements consist of the major registers and their associated control elements, the timing generators for the computer system, the manual controls, and the special program feature controls (data break control, program interrupt control, I/O skip, I/O trap, etc.).

3.3.1 Registers

3.3.1.1 Accumulator - The AC is the major arithmetic register of the CP and is involved in most of the mathematical, logical, and I/O transfer operations performed by the computer. This register consists of 18 Type B210 Accumulator FLIP CHIP modules at locations HJ2 through HJ19. The AC has a storage

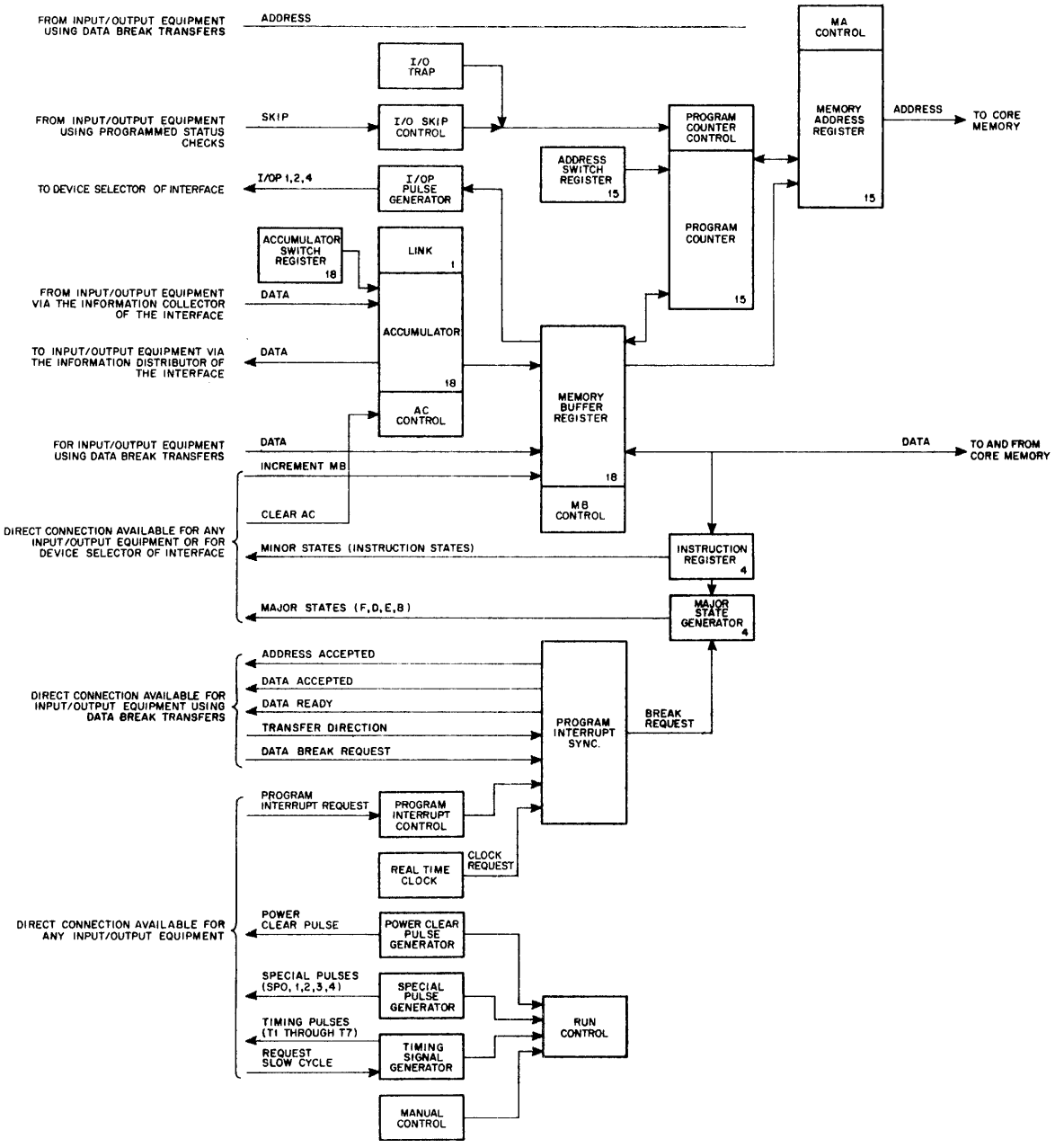


Figure 3-2 Processor Detailed Block Diagram

capacity of 18 bits. In programmed operation each flip-flop of the AC can be individually set or cleared by means of gated signals from other registers or from external equipment. The flip-flops can also be set (but not cleared) by means of the ACCUMULATOR switches on the operator console. The AC may also be cleared collectively, or its contents incremented by 1, complemented, rotated, or shifted right or left. An indicator on the operator console shows the status of each flip-flop in the register.

Each Type B210 module is a double-height module containing one buffered-output flip-flop, a carry pulse amplifier, and all the required transistor gating elements. A positive pulse from a gating circuit sets or cleares the flip flop; the gates are conditioned by negative levels and are triggered by negative pulses.

All bits of the accumulator are cleared collectively by a 0→ AC pulse applied to input terminal HV of a transistor gate connected to the direct clear input (HS) of the flip-flop.

Each bit of the AC may be individually set by a positive pulse from the information collector applied to terminal HU, which is connected to the direct set terminal (HT) of the flip-flop. An unused transistor gate permits a bit to be set by application of a negative pulse to terminal JL.

A pair of transistor gates to which the RAR pulse is applied, (at terminals HJ and HN), rotate right operations. These gates set or clear the associated flip-flop according to the status of the adjacent flip-flop of greater significance. The (1) level of this flip-flop is applied to terminal HH, and the (0) level to terminal HM.

A similar pair of gates to which the RAL pulse is applied, (at terminals HL and HR), rotate left operations. The (1) level (terminal HK) and the (0) level (terminal HP) of the adjacent flip-flop of less significance condition these gates.

Each bit of the AC may be cleared by a 0 in the corresponding bit of the MB. The MB (0) level is applied to terminal JH and clears the AC flip-flop when an MB0→ AC pulse is applied to terminal JF.

Each bit of the AC may be set by a 1 in the corresponding bit of the accumulator switch register. The (1) level from the corresponding ACCUMULATOR switch is applied to terminal JK, and the ACS1 pulse to terminal JJ.

Complementing is accomplished by applying a positive pulse to both the direct set and direct clear inputs of the flip-flop, through isolating diodes. Complementing is performed by any one of the following:

a. A negative C→ AC pulse is applied to terminal JT; a transistor inverts the pulse.

b. A positive pulse from the XOR NAND gate; this gate is conditioned by an MB (1) level applied to terminal JV, and is triggered by a negative XOR→ AC pulse applied to terminal JU. The output of the gate complements the AC flip-flop.

c. By a carry pulse from the adjacent AC bit of less significance. The negative carry pulse is applied to terminal JP and is inverted by a transistor.

Carry pulses propagate to the adjacent bit of greater significance as they develop at the type B210 Pulse Amplifiers. A carry from bit ACx to bit ACx-1 is generated under the following conditions:

a. When bit ACx contains a 1, and a carry pulse is received from bit ACx+1. The negative ACx(1) level conditions terminal FD of a NAND gate; the incoming carry complements bit ACx and triggers the NAND gate. The output of the gate triggers the carry pulse amplifier which transmits a carry pulse to bit ACx-1.

b. During an ADD or TAD instruction, an XOR operation is first performed between the MB and the AC. After the XOR operation, an AC CRY pulse is applied to all bits of the AC at terminal FR of a NAND gate. If the level inputs of this gate are conditioned by an MBx(1) level applied to terminal FV and an ACx(0) level applied to terminal FE, the AC CRY pulse causes the gate to trigger the carry pulse amplifier and a carry is transmitted to bit ACx-1. The resulting changes of state in flip-flops of greater significance may result in additional carries being propagated as described in a. (above).

3.3.1.2 Link - The Link (L) is an extension of the AC and is used for data overflow. The link consists of a single Type B210 Accumulator module. Storage capacity is a single bit. The link is capable of the same functions as the AC and can be operated independently of, or in conjunction with, the AC. An indicator on the operator console shows the status of the link.

Any one of the following conditions clears the link:

a. A BGN pulse at time SP1 of any key operation.

b. A microprogrammed rotate right command, if bit AC17 is 0.

c. A microprogrammed rotate left command, if bit AC0 is 0.

d. A microprogrammed clear link command (bit MB6 is 1) at time T5 of the computer cycle.

Any one of the following conditions sets the link:

a. An EAE SET L pulse originating in the extended arithmetic element.

b. A microprogrammed rotate right command, if bit AC17 is 1.

c. A rotate left command, if bit AC0 is 1.

d. Timing pulse TP1 of the computer cycle, if the AC overflowed during the previous cycle.

The link is complemented:

a. By an AC0 CRY (overflow) during a EAE multiply or divide operation.

b. By a TAD CRY pulse generated by an AC overflow during 2s complement addition; by a microprogrammed complement link command in an operate instruction; or by a complement link command originating in the EAE.

3.3.1.3 Program Counter - The PC determines the core memory address from which the next instruction is fetched. This register consists of 15 Type B201 Flip-Flops at locations F18 through F32 and 7 Type B620 Carry Pulse Amplifiers at locations 1H21 through 1H27. The PC has a storage capacity of 15 bits. In normal (nonextended) operations, only 13 of these are used. The 13 flip-flops containing these 13 least significant bits can be individually set either by gated signals in automatic operation or by the ADDRESS switches in manual operation. The PC can only be cleared collectively. The inclusion of complementing gates and carry pulse amplifiers permits the contents of the PC to be incremented by 1 injected into the least significant bit. An indicator on the operator console shows the status of each flip-flop.

3.3.1.4 Memory Address Register - The (MA) contains the address of the core memory cell currently selected for reading or writing. This register consists of 15 Type B201 Flip-Flops at locations C18 through C32, and has a storage capacity of 15 bits. Each flip-flop of the MA can be individually set by gated signals from other registers but can only be cleared collectively. An indicator on the operator console shows the status of each flip-flop.

3.3.1.5 Memory Buffer Register - The (MB) serves as a data buffer between the processor and the core memory. This register consists of 18 Type B201 Flip-Flops at locations E2 through E19 and 9 Type B620 Carry Pulse Amplifiers at even-numbered locations 1D2 through 1D18, and has a storage capacity of 18 bits. The register flip-flops can be individually set by gated signals but can only be cleared collectively. The circuits of the MB are similar to that of the MA with the addition of the pulse amplifiers and complementing gates which allow the contents of the MB to be incremented by 1, injected into the least significant bit. An indicator on the operator console shows the status of each flip-flop.

3.3.1.6 Major State Generator - Four NAND gates compose the multistate device which generates the four major state levels: a Type B115 FLIP CHIP module at location K18 contains three, and another similar module at location L17 contains the fourth. When disabled, each NAND gate produces a negative level at its output terminal; when fully enabled by three negative levels, the gate produces a ground output level. The gates are so interconnected that the output signal of each gate is applied to one input terminal of each of the other three gates. Thus, if the fetch produces a ground output, this signal disables the other three gates, so that each produces a negative output. These three negative output signals are returned to the input terminals of the fetch gate to maintain it in the fully enabled state. If a positive pulse is now applied to the output of the execute gate, this pulse keeps the defer and break gates disabled, but also disables the fetch gate. Terminals F and E of the execute gate remain enabled by the negative levels from the defer and break gates, but terminal D makes a transition from ground to −3v when the fetch gate is disabled. The execute gate is now enabled by three negative input levels, so that its ground output level is maintained after the setting pulse is ended. Two Type R602 FLIP CHIP modules in locations L18 and K19 provide setting pulses for the multistate device. Each module contains two pulse amplifiers, which produce a standard positive 100-nsec pulse. Each pulse amplifier is provided with two DCD gates enabled by the combination of a ground level and a positive pulse. In principle, any state can be entered from any other state; however, the major state gating makes certain necessary modifications to this principle.

During the execution of programmed instructions, the conditions established during any given cycle determine the major state for the next cycle. At time T7, those conditions are implemented by combining an F SET, D SET, E SET, or B SET level with timing pulse TP7 to produce a pulse that sets the multistate device. However, when starting a program or performing a manual operation, other means may establish a fetch or execute state under one of the following sets of conditions:

a. When the START key is depressed, the positive START level generated by the key circuits is combined with timing pulse SP1 of the key cycle. The resulting pulse triggers pulse amplifier PA1 in module L18 setting the multistate device to the fetch state.

b. A PI1 → MA pulse, inverted in module L30, triggers pulse amplifier PA2 of module L19 and establishes a fetch state.

c. When a program is running in the trap mode, and an illegal XCT instruction is trapped, a positive TRAP FLAG (0) level (produced only when the TRAP FLAG flip-flop is set) is combined with the XCT CY (1) signal. This establishes a fetch state immediately, to avoid implementing the illegal instruction.

d. During normal operation, an F SET level is combined in a DCD gate with timing pulse TP7 INVTD B; and the resulting output of the gate triggers pulse amplifier PA1 of module L18 to establish a fetch state.

The positive F SET level is generated by a NAND gate in module L21 and appears at output terminal H of the gate. When negative $\overline{\text{D SET}}$, $\overline{\text{E SET}}$, and $\overline{\text{BK RQ}}$ levels enable all three inputs, the ground F SET level appears at the output. An F SET NEG level is produced at terminals of module K22. The $\overline{\text{D SET}}$ level indicates that the current instruction does not contain an indirect address which requires a defer cycle to follow the fetch. The $\overline{\text{E SET}}$ level indicates that the current cycle is not a defer cycle which requires an execute cycle to follow it. The $\overline{\text{BK RQ}}$ level indicates that no I/O device needs servicing.

An execute state is established under the following conditions:

a. When any operation key other than the START key is depressed, a negative $\overline{\text{START}}$ level derived from the key circuits enables a NAND gate in module L22 (B3, 24). When the BGN pulse of the key cycle is added, the gate triggers pulse amplifier PA2 of module L18 and establishes the execute state.

b. During programmed operation, an E SET level conditions one input of a DCD gate; and timing pulse TP7 INVTD causes the gate to trigger the associated pulse amplifier and establish the execute state.

c. When a positive FORCE E SET pulse is generated during execution of certain EAE instructions.

One of three NAND gates located in modules L21, K20 and M19 generates the ground E SET level which appears at terminal K20U if all of the following conditions are met: the current cycle is operating in the fetch state; the operation code stored in the IR produces an $\overline{\text{IA3}}$ level (indicating that the instruction is not a single-cycle law, operate, or IOT instruction); and bit MB4 is 0 (indicating that the instruction contains the direct address of the operand). The ground E SET level appears at terminal J21F if the current cycle is operating in the defer state and the operation code produces an $\overline{\text{IA3}}$ level. The ground E SET level appears at terminal M19R if the RPT flip-flop is set (during a readin operation).

A defer state is established during the fetch cycle of any memory reference instruction or JMP instruction which contains a 1 in bit 4. The negative F level and MB4(1) levels are combined in NAND gate JKL of module L21, and the output of the gate is inverted in inverter PRS of module L20. The output of this inverter and the output of NOR gate NPR of module L21 are both applied to inverter

TUV in module L20. Note that both the NAND gate and the NOR gate must give negative outputs to produce the ground D SET level at terminal L20U. The NOR gate gives a negative output when the IA3 level from the IR decoder is at ground (this condition is not fulfilled when the IR contains 60 JMP, 64 EAE, 70 IOT, or 74 OPR/LAW), or when the $\overline{IB0}$ level is at ground (this condition is equivalent to an IB0 assertion and occurs when a JMP code is held in the IR).

A break state is established if a break request conditions NAND gate KLMN of module L21, provided that neither a D SET nor an E SET level has already been established for the following cycle. These conditions can be fulfilled at time T7 of the fetch cycle of an OPR, LAW, IOT or directly addressed JMP instruction; during the defer cycle of an indirectly addressed JMP instruction; during the execute cycle of any multicycle instruction; and during a break cycle.

3.3.1.7 Instruction Register - The IR flip-flops, together with the input gates and the output decoder appear at the right of engineering drawing 7. The output pulse of pulse amplifier RNPM in module L16 clears simultaneously all four flip-flops. This pulse amplifier is triggered by any one of the following conditions:

a. A BGN pulse applied to inverter input terminal K15D (C5,7).

b. A timing pulse T1 applied to NAND gate NPR of module K16, when the gate is conditioned by an F (fetch) level.

c. A timing pulse T1 applied to NAND gate JKL of module K16, when the gate is conditioned by a B (break) level.

d. A timing pulse T2 applied to NAND gate DEF of module K16, when the gate is conditioned by an E · XCT level. (The E · XCT level is generated by combining the IA2 and IB0 levels from the IR decoder with the E (execute) level in NAND gate RSTU of module L17. The output of the gate is inverted and the E · XCT level appears at terminal K17U, provided that the trap flag is not set.)

A 4-bit operation code may be set into the IR in one of the following ways:

a. When an F level conditions the four input gates in module K13, a binary 1 pulse from any one of sense amplifier SA0 through SA3 sets the corresponding IR flip-flop to 1.

b. During execution of a CAL instruction, the 20→ MA pulse generated in the MA control is applied to inverter input terminal L15D. The inverted pulse sets flip-flop IR2 to 1, thereby substituting a JMS (octal 10) operation code for the CAL (octal 00) code held in the IR.

c. During a deposit, deposit next, or read paper tape operation, a DP+DPN+READ-IN+RPT(1) level conditions NAND gate STU in module L12. The gate is triggered by timing pulse SP(2) of the key cycle and sets operation code 04 (DAC) into the IR by setting flip-flop IR3 to 1.

d. During an examine or examine-next operation, an EX+EXN level conditions NAND gate LMN in module L12. This gate is triggered by timing pulse SP2 of the key cycle and sets operation code 20 (LAC) into the IR by setting flip-flop IR 1 to 1.

The operation code is decoded by two sets of NAND gates and inverters. The gates of module K14 and the inverters of module K15 decode the outputs of flip-flops IR0 and IR1. Gating levels IA0 through IA3 and $\overline{IA3}$ appear at terminals K15J, M, R, U, and T, respectively. The gates of module L14 and the inverters of module L15 decode the outputs of flip-flops IR2 and IR3. Gating levels IB0 through IB3 appear at inverter output terminals L15J, M, R, and U, respectively.

3.3.2 Timing

Each arithmetical and logical operation within the PDP-7 system is initiated by a command pulse derived from the combination of 1 or more condition-indicating levels and 1 of 5 special purpose timing pulses or 1 of 14 memory cycle timing pulses. There is a considerable variation in the time required to perform the various machine operations because of the varying number of logic elements involved. It is necessary, therefore, that these timing pulses be spaced at appropriate (but not equal) intervals. For this reason, the PDP-7 does not contain a crystal clock or other generator of constant-frequency signals. Instead, timing pulses are generated by two chains of pulse amplifiers, each amplifier being separated from the next by a delay line or one-shot, which produces the desired interval between the two associated timing pulses. Thus, a pulse or level transition applied to the first element is propagated down the chain, generating as many standard-width timing pulses as there are delay/pulse amplifier pairs in the chain. If the output pulse from the last pair is returned, through a suitable delay, to the input of the first pair, the pulse train becomes self-maintaining and ceases only when the circular path is broken at some point.

3.3.2.1 Power Clear Pulse Generator (3) - During the power turn-on sequence, the power clear pulse generator produces repeated PWR CLK (power clock) pulses at a repetition rate of approximately 200 kc. These pulses clear the RUN flip-flop to establish correct initial conditions. The PWR CLK pulses are

combined with the RUN(0) level to produce positive and negative PWR CLR (power clear) pulses, which are supplied to the reader control, punch control, and to the LUO (line unit out) buffer of the Teletype control. The PWR CLR pulses are also supplied to the interface connectors, where they are available to clear the registers of I/O devices in order to establish correct initial conditions.

In the power turn-on sequence, the power supplies which provide +10v and −15v for the CP logic are energized through the fast-on, delay-off contact K3 of the Type 832 Power Control. The memory power supplies are energized through the delay-on, fast-off contact K2 of the power control, which provides a delay of 3 to 5 sec. At the beginning of this delay period, when the CP is first turned on, the potential of terminals X and Y of the Type 1404 clock is near ground, thereby enabling the clock. However, these terminals are connected through a resistor to the delayed −15v memory supply. When memory power is turned on, the potential of terminals X and Y approaches −15v, thereby again disabling the clock. The clock is enabled for a period of approximately 5 sec. The negative pulses appearing at terminal E of the clock are inverted in module K22, (3), and the inverted pulses are applied to one of the DCD gates of the RUN flip-flop to clear it. Two NAND gates in module E31 are conditioned by the RUN (0) level (terminals E and K); and, when triggered by the PWR CLK pulses at terminals D and J, these gates each give an output pulse. The pulse appearing at terminal F triggers one pulse amplifier in module E28, which produces the PWR CLR NEG pulse. The pulse appearing at terminal L of module F31 triggers a second pulse amplifier in module D28, which produces the PWR CLR POS pulse.

3.3.2.2 Special Pulse Generator (5) - The special pulse generator provides the special pulses required for timing events initiated by the manual keys and switches on the operator console. These pulses consist of the BGN (begin) pulse, used for clearing registers prior to operation, and five timing pulses designated SP0 through SP4. The special pulse generator consists of a Schmitt trigger and a chain of five pulse amplifiers, each pair of pulse amplifiers being separated by a one-shot delay.

Initial excitation of the special pulse generator takes place when any one of the manual keys, except the STOP key, is operated. Key operation generates two negative levels designated KEY MANUAL and $\overline{\text{CONT}}$ (not continue), except in the case of the CONTINUE key, which generates only the KEY MANUAL level. The KEY MANUAL level causes the Schmitt trigger in module K31 (Type W501 FLIP CHIP) to change state, thereby providing initial excitation of the special pulse timing chain. The positive-going level transition appearing at terminal F of the Schmitt trigger is applied to terminal H of module L30, where it triggers a pulse amplifier through a DCD gate. The output of this pulse amplifier is a 100-nsec pulse designated SP0, which clears the RUN flip-flop (6). The SP0 pulse is also applied to input terminal E of delay module L29. After 10 μsec, a positive level transition appears at terminal M of the delay module and triggers the pulse amplifier, which provides pulse SP1. Thereafter, pulses SP2, SP3, and SP4 appear at 2-μsec intervals. Pulses SP1 through SP4 are 70 nsec wide positive pulses,

which strobe registers or transfer information within the CP. When a key operation is completed during special time states SP0 through SP4, timing pulse SP4 is allowed to die out; and no further action occurs until a new KEY MANUAL level is generated. In key operations (other than read paper tape) which require one or more computer cycles for completion, timing pulse SP4 is NAND combined with the RPT(0) level in module M14. The pulse output from the gate triggers a DCD gate in module M28, which provides initial excitation for the CP timing signal generator. If the REPEAT switch is turned on, the REPEAT level is combined with the KEY MANUAL level to trigger the Type R401 Integrating One-Shot in module K30. After an interval determined by the SPEED controls on the console, this one-shot reverts to its stable state and triggers the pulse amplifier that generates pulse SP0, thereby causing the key operation just completed to be repeated.

The BGN pulse is generated by combining the SP1 pulse with the $\overline{\text{CONT}}$ level in module L25. The positive pulse appearing at terminal F of this module is applied to terminal E of module M17, where it triggers a pulse amplifier. The output of this pulse amplifier is a negative BGN pulse, appearing at terminal H, which clears the special mode flip-flops (TRAP FLAG, I/O TRAP, RPT, XCT CY), the IR flip-flops, and the program interrupt sync flip-flops.

3.3.2.3 Timing Signal Generator - Like the special pulse generator, the timing signal generator consists essentially of a chain of pulse amplifiers separated by delay networks. However, the gating which controls excitation (or regeneration) of the first pulse is somewhat more complex. Provision is made for a slow cycle in which additional delays are inserted between timing pulses TP6 and TP7 of one cycle and TP1 of the following cycle.

After a key cycle, entry to the main computer timing cycle is obtained by NAND-combining timing pulse SP4 with the RPT(0) level (the RPT flip-flop having been cleared by the BGN pulse in time state SP1). The positive output pulse from the NAND gate (module M14) is applied to terminal N of module M28. This module consists of a Type R601 Pulse Amplifier having six DCD gate inputs, of which five are used for isolation or selection purposes. The output of the pulse amplifier is a standard 100-nsec positive pulse which triggers the first amplifier/delay pair of the timing chain.

Each amplifier/delay pair of the timing chain consists of a Type B360 FLIP CHIP module containing a pulse amplifier and a delay line. In the PDP-7 system, the module is so connected that the pulse amplifier provides a standard 40-nsec negative pulse, which is available as a timing pulse of the TP1 through TP7 series. The output pulse is also applied to the delay line, which provides a delay adjustable between 20 and 250 nsec, with a resolution of 0.25 nsec. The delayed negative pulse is inverted to provide a positive trigger pulse for the next pulse amplifier. The 70-nsec negative timing pulses in the series T1 through T7 are obtained from Type W607 modules, each containing three pulse amplifiers. The input trigger for each pulse amplifier is obtained by inverting the corresponding timing pulse of the TP series.

During a normal computer cycle, the TP6 pulse (delayed by 240 nsec) is routed through a Type B104 Inverter in module M21. This inverter gate is conditioned by a $\overline{\text{SLOW CYC}}$ level, and its positive output pulse triggers the succeeding pulse amplifier to produce the TP7 pulse. The TP7 pulse returns to the first pulse amplifier of the chain through a 150-nsec delay and a series of gates. The next cycle begins immediately, if the following conditions are met: Inverter input terminal M21K is conditioned by a negative $\overline{\text{STOP CP TC}}$ level (indicating that no EAE operation is in progress); and inverter input terminals M21E and N15T are enabled by a negative $\overline{\text{SLOW CYC}}$ level and a negative RUN (1) level, respectively. If these conditions are satisfied, both the level input (H) and the pulse input (J) of a DCD gate in module M28 are enabled; and the delayed TP7 pulse triggers the associated pulse amplifier to initiate the generation of pulse TP1 of a new cycle. If EAE operations are in progress, the inverter input at M21K may be disabled by a positive STOP CP TC level; and the processor is then temporarily halted. The processor is restarted when a positive START CP TC pulse arrives at input terminal T of another DCD gate, which is conditioned by a positive RUN (1) level.

During a slow cycle, the inverter in module M21 is disabled. The TP6 pulse then travels through a second inverter of module M21 (input terminal P), which is conditioned by the SLOW CYC level. The positive output pulse from the inverter is applied to the one-shot in module M20. This one-shot has a DCD gate input, and the delay is adjustable over the range 400 nsec to 4 μsec. The normal reentry into the timing chain is disabled by the positive $\overline{\text{SLOW CYC}}$ level, which appears at inverter input terminal M21E. Instead, pulse TP7 is inverted in module L28; and the pulse amplifier in module K19 produces a TP7 INVTD (B) pulse, which triggers a Type R302 One-Shot in module M20. A positive SLOW CYC level conditions the DCD input gate of this one-shot, and, at the conclusion of the delay period, the level transition which appears at output terminal M20M initiates generation of pulse TP1 of a new cycle.

Every IOT instruction fetched from memory causes the minor state generator to produce negative IA3 and IB2 levels. These levels go to input terminals R and P, respectively, of module L23 (C4,6) where they are NAND combined with the I/O TRAP (0) level. Thus, provided that the I/O TRAP flip-flop has not been set, the gate gives an output which is inverted and appears as a negative IOT level at terminal K23K (C4,6). Each I/O device that requires a slow cycle must generate a negative $\overline{\text{RQ SLOW CYC}}$ level. This level is NAND combined with the IOT level in module L22 (D5, 6) to produce the positive SLOW CYC and negative $\overline{\text{SLOW CYC}}$ levels. The inverter in module K22 (D6, 6) in turn produces the negative SLOW CYC and positive $\overline{\text{SLOW CYC}}$ levels. These four levels control the gates that determine the signal paths through the timing chain for normal and slow cycles. The total delay of the slow cycle is factory adjusted to accommodate the slowest I/O device in use.

When the tape reader is loading information into memory, each tape character is read into the reader buffer as the result of an operation in the READ-IN mode which utilizes timing pulses SP0 through SP4 of one key cycle. However, the reader buffer assembles an 18-bit computer word by storing three type characters successively in different sections of the buffer. The information transfer between reader

buffer and processor must be delayed until the reader buffer is full. During readin, therefore, the RUN flip-flop is not set during the key cycle. Instead, a negative KEY MANUAL level (generated by releasing the $\overline{\text{KEY MANUAL B}}$ key after initiating the operation) and a negative RPT(1) level condition the NAND gate in module M14 (D2,22). When the reader starts to read the third tape character, the RD FLAG flip-flop is set, indicating that the reader is ready to transfer information, and the negative RD FLAG level conditions the third input of the gate. The last level to appear causes a positive-going level transition at terminal M14H, thereby initiating a timing cycle during which the complete word is transferred from the reader buffer into the processor. When the transfer is complete, the reader flag is reset, and the timing signal generator is halted until another word is ready for transfer.

3.3.2.4 Run Control (6) - The RUN flip-flop controls the continuous succession of normal computer timing cycles. When the flip-flop is set to 1, and there is no slow cycle or stop timing request, timing pulse TP7 of the current cycle (delayed by 150 nsec) is permitted to reenter the timing chain and generate timing pulse TP1 of the next cycle. When the RUN flip-flop is reset to 0, it disables a gate in the reentry path and stops the computer, unless other conditions permit a new cycle to be initiated. (Refer to the description of the timing signal generator for details.) The program may halt the CP, but a manual START or CONTINUE operation must then restart it.

The RUN flip-flop is an unbuffered flip-flop contained in a FLIP CHIP Type R201 module which also contains two DCD gates for clear inputs and three for set inputs. The flip-flop is reset to 0 by the following events:

a. When power is turned on after a shutdown, PWR CLK negative pulses are inverted in module K22 and applied to a DCD clear input (terminal K26E) in order to establish initial conditions.

b. When any console key is depressed to initiate an operation, the SP0 timing pulse is applied to direct clear input terminal K26K, thereby causing any operation already in progress to be halted at the end of the current memory cycle.

c. A positive RUN STOP level is generated by the STOP, SINGLE STEP, or SINGLE INSTRUCTION key. This signal appears at terminal K26J of a DCD gate. Timing pulse T5 is inverted in module L26, and the inverted pulse, applied to terminal K26H, triggers the gate and clears the RUN flip-flop.

d. A positive HLT pulse arrives at terminal K26E to trigger a DCD gate and clear the RUN flip-flop. The HLT command is generated by NAND combination of the I/O TRAP(0) level, an MB12(1) level, and an IOP 1 pulse. The MB12(1) level is derived from the execution of

an OPR instruction containing a HLT micro-instruction. The RUN flip-flop is cleared at time T5. The CP halts after time T7 of the same cycle.

The RUN flip-flop is set under the following conditions:

a. Depressing the START or CONTINUE key generates a negative START+CONT level, which is NAND combined in module L25 with the SP3 timing pulse. The positive pulse produced by the gate is applied to terminal K26S, where it triggers a DCD gate and sets the RUN flip-flop.

b. During a readin operation, a positive RPT(1) level conditions terminal K26V of a DCD set gate. The pulse input of this gate (K26U) is triggered when a RDR HOLE 7 level is NAND combined with timing pulse T5 of the cycle in which a hole 7 was detected. (A hole 7 indicates that the processor is to interpret and execute the last word read.)

3.3.2.5 I/O Pulse Generator (5) - Timing pulses for the control of I/O devices are generated in modules M30 and M31. Module M30 is a FLIP CHIP Type B115 containing three NAND gates; the output of each gate triggers an associated pulse amplifier in module M31 to produce a standard negative 40-nsec pulse. Any instruction of the IOT class generates a negative IOT level, which is applied to all three NAND gates. The subsequent generation of I/O pulses depends on the state of memory buffer bits MB15, MB16, and MB17. If bit MB15 is 1, an IOP 4 pulse is generated at time T1 of the computer cycle; if bit MB16 is 1, an IOP 2 pulse is generated at time T7; if bit MB17 is 1, an IOP 1 pulse is generated at time T5. These pulses are routed to the device selector; there they are combined with device selection levels to generate IOT command pulses that control the operation of the selected I/O device or trigger control gates in the CP.

3.3.2.6 Manual Controls - The manual controls provide means of energizing and de-energizing the computer, selecting modes of operation, manually inserting data into registers and core memory, and visually examining the status of the most important registers. Wiring connections to the keys and switches on the operator console panel are shown on engineering drawing 3. The logic for gating signals produced by the keys and switches is also shown on engineering drawing 3.

3.3.2.7 Interlock and POWER Switches - One deck of the key switch is connected in parallel with the POWER switch and is closed when the switch is in the locked position. Thus, with the key switch in the locked position, it is impossible to ruin a program because accidentally turning off the POWER switch does not interrupt the primary power circuits. To shut down the computer, the key switch must be placed in the unlocked position and the POWER switch in the off position. A second deck of the lock switch

supplies either ground or −15v to the key and mode switches. In the locked position, the key switch grounds all key switches to disable them thereby preventing accidental interference with a program that is running.

3.3.2.8 Key Circuits - When the computer is energized and the lock switch is in the unlocked position, operating any of the keys or turning on the SINGLE STEP, SINGLE INSTRUCTION, or REPEAT switches supplies −15v to a terminal on connector 2B29 or 2B32. The gating circuits shown on engineering drawing 3 combine key signals to generate various levels. These levels start the special pulse generator and condition control gates, as necessary, to cause the event sequences appearing in the flow diagram included on the drawing.

3.3.2.9 Indicator Circuits - Indicators on the operator console are 28v incandescent lamps driven by Type 4903 Light Bracket Assemblies or Type 4904 Short Light Bracket Assemblies. These assemblies contain a number of transistor switches, each connected between an indicator and ground. One side of each indicator is connected to the −15v supply. A common ground potential is connected to the emitter of each transistor through parallel-connected diodes, which provide the appropriate base-emitter bias. Each transistor switch is turned on by a negative signal level derived from a flip-flop and connected to the base through a resistor. When a flip-flop is in the 0 state, it supplies a ground potential that cuts off the transistor switch and extinguishes the associated indicator lamp. When a flip-flop is in the 1 state, it supplies a negative potential to the transistor switch; and the indicator lamp lights. The potential applied to a lighted indicator lamp is approximately 14v, which provides adequate visibility while ensuring very long lamp life.

3.3.3 Register Controls

3.3.3.1 Accumulator Register Control (9) - The command pulses which clear the AC; propagate carries; cause rotation; initiate the transfer of information from another register into the AC; and set, clear, or complement the link are all generated in the logic circuits shown on engineering drawing 9. These logic circuits also generate twelve conditioning levels and two timing pulses, which primarily control the conditions under which a command pulse is generated. Some of these levels and pulses, however, are also transmitted to other register controls.

Pulse amplifier circuit RNPM in module K2 generates the $0 \rightarrow$ AC command pulse and clears all the flip-flops of the AC simultaneously. Any one of the following conditions clears the AC:

a. A BGN pulse, generated at time SP1 of any manual operation except STOP or CONTINUE, is applied to terminal L2E. The inverted pulse appearing at terminal L2D triggers the pulse amplifier.

b. During a read paper tape operation, the RPT(1) level conditions AND gate UV of module L2. Timing pulse SP4 of the key cycle triggers the gate, and the inverted pulse appearing at terminal L2D triggers the pulse amplifier.

c. During the execution of a LAW instruction, a negative OP LAW level conditions AND gate PR of module L2. Timing pulse T5 triggers the gate and causes clearance of the AC. The OP LAW level is generated by combining a 1 on bit 4 of the instruction word with the IA3 and IB3 levels produced by the IR decoder.

d. An operate class instruction microprogrammed to clear the AC contains a 1 in bit 5 of the instruction word. The buffered output of the MB5 flip-flop conditions AND gate KL of module L2. Timing pulse OPR triggers the gate and causes clearance of the AC. The OPR timing pulse is generated by NAND-combining the MB4(0) level with the IA3 and IB3 levels from the IR decoder in module L12. The output of the NAND gate is inverted to produce a negative OPR level which conditions a further NAND gate (terminals JKL of module K8). This gate is triggered by timing pulse T4 and causes the pulse amplifier circuit EHF in module H8 to generate the OP1 pulse.

e. An EAE CLA (EAE clear accumulator) level, generated in the EAE, conditions AND gate ST of module L2. The gate is triggered by timing pulse T4 and causes clearance of the AC.

f. If the I/O trap is disabled, it is possible to microprogram any IOT instruction to clear the AC during time T5 by inserting a 1 in bit 14 of the instruction. The IA3 and IB2 levels produced by the IR decoder are combined with the I/O TRAP(0) level in NAND gate NPRV of module L23 (C4, 6). Two inverters in module K23 invert the output of the NAND gate. The output of one of these inverters is an IOT level; the output of the other is combined with the MB14(1) level in inverter PRS of module K23 (D4, 6). The output of this inverter is a negative IOT. CLA level, which conditions AND gate NM of module L2 in the AC control (A5, 9). This gate is triggered by timing pulse T5 and causes clearance of the AC.

g. During the execute cycle of an LAC instruction, the E level from the major state generator is combined with the IA1 level from the IR decoder in module K9 to produce an E · IA1 level.

This level is further combined with the IB0 level from the IR decoder in module K9 to generate an E · LAC level, which conditions AND gate JH of module L2. This gate is triggered by timing pulse T1 of the execute cycle and causes clearance of the AC.

The XOR → AC command pulse causes the complementing of each bit of the AC that corresponds to an MB bit in the 1 state. If the AC is cleared, the effect simply transfers the contents of the MB into the AC. If the AC already contains a binary number and the propagation of carries does not follow the XOR transfer, an exclusive OR operation is performed between the contents of the MB and the contents of the AC; i.e., AC bits initially containing a 1 change to the 0 state if they correspond to MB bits containing a 1. If the AC contains a binary number, and the XOR transfer is followed by the propagation of carry pulses and then by an end-around carry of an overflow from bit AC0, the contents of the MB are added to the contents of the AC in 1s complement arithmetic. If the overflow from bit AC0 is set into the link instead of into bit AC17, the contents of the MB are added to the contents of the AC in 2s complement arithmetic. Any one of the following conditions generates the XOR → AC pulse:

a. An XOR pulse originating in the EAE is applied to terminal L3E and initiates an XOR command.

b. During execution of any LAW instruction, a negative OP LAW level conditions AND gate MN of module L3. The gate, triggered by timing pulse T6, initiates the XOR command.

c. During the execute cycle of a LAC, XOR, ADD, or TAD instruction, a negative E · IA1 level conditions AND gate HJ of module L3. The gate, triggered by timing pulse T3, initiates an XOR command.

d. During the execute cycle of a SAD instruction, a negative E · SAD level is generated by combining the E level from the major state generator with the IA2 and IB3 levels from the IR decoder in NAND gate RSTU of module K12. The output of the gate, inverted, is the E · SAD level and conditions AND gates PR and KL of module L3. Gate KL, triggered by timing pulse T3, initiates an XOR command; a second XOR command is initiated when timing pulse T6 triggers gate PR in module L3.

Pulse amplifier circuit FDEC in module K5 generates the AC CRY (AC carry) command pulse. During the execute cycle of either a TAD or an ADD instruction, the E · TAD or E · ADD ground level is applied to NOR gate NPR of module L5 to generate the E · TAD + ADD negative level. This level

conditions NAND gate DEF of module L4. Timing pulse T4 triggers the gate, and the positive pulse appearing at terminal L4F triggers the pulse amplifier which generates the AC CRY pulse. A positive EAE CRY pulse originating in the EAE may also trigger the pulse amplifier.

Pulse amplifier circuit FDEC in module K3 generates the END CRY (end-around-carry) command which causes an overflow from bit AC0 to be added to bit AC17, with further carry pulses as necessary. A negative E · ADD level conditions NAND gate TUV in module L4. If bit AC0 contains a 1 before the carry operation, and changes to 0 as the result of carry pulses from less significant bits, an AC0 CRY pulse is generated. This pulse, after inversion, triggers the pulse amplifier STU in module K8, and the output pulse from this amplifier triggers NAND gate TUV in module L4, thereby initiating generation of the END CRY pulse. The END CRY pulse complements bit AC17, further carry pulses being generated as necessary.

Pulse amplifier circuit RNPM in module K3 generates the TAD CRY (2s complement addition carry) command pulse which complements the link whenever one of the following conditions occurs:

a. An EAE CML (EAE complement link) command pulse originating in the EAE triggers the pulse amplifier that generates the TAD CRY pulse.

b. An OPR instruction, microprogrammed to complement the link, contains a 1 in bit 16. The MBB16(1) level conditions NAND gate TUV in module L5 (B5, 9), and an OP 2 pulse triggers the gate. A TAD CRY pulse is then generated at time T7 of the computer cycle.

c. During the execute cycle of a TAD instruction, a negative E · TAD level conditions NAND gate NPR in module L4 (B6, 9). If the AC overflows, this gate is triggered by the AC0 CRY (B) pulse and initiates generation of the TAD CRY pulse.

Pulse amplifier circuit RNPM in module H5 generates the C → AC command pulse. This pulse complements each individual bit of the AC and occurs when an EAE CMA (EAE complement AC) command pulse, originating in the EAE, triggers the pulse amplifier. The C→ AC pulse also occurs at time T7 during the execution of an OPR instruction which is microprogrammed for a CMA operation by the insertion of a 1 in bit 17. The MB17(1) level conditions NAND gate JKL in module L4 (B6, 9), and an OP 2 pulse triggers the gate at time T7. The OP 2 pulse is generated by NAND-combining the negative OPR level with timing pulse T7 in gate NPR of module L8 (C2, 9), and applying the resulting pulse to pulse amplifier LNM in module K8.

The RAR and RAL command pulses are generated at terminals N and D, respectively, of pulse amplifier module K4. A NAND gate, conditioned by an MBB13(1) level (for RAR) or an MBB14(1) level (for RAL) triggers each of the two pulse amplifiers. An AC ROTATE pulse at time T5 strobes these gates initiating generation of the RAR or RAL pulse. If the instruction word contains a 1 in bit 7, the MBB7(1)

level conditions a NAND gate which is triggered by an OP1 pulse at time T7 and produces an additional AC ROTATE pulse. Thus, one RAR or RAL pulse is generated at time T5 for a 1-place rotate operation; if a 2-place rotate is microprogrammed, a second RAR or RAL pulse occurs at time T7. Rotate command pulses originating in the EAE are applied to the input terminal of the RAR or RAL pulse amplifier (terminals K4R and K4F, respectively) and initiate generation of the RAR or RAL command pulses.

Pulse amplifier circuit RNPM in module K6 which appears at terminal K6N generates the MB0 → AC command pulse. This command pulse causes MB bits in the 0 state to set the corresponding bits of the AC to the 0 state. During the execute cycle of a logical AND instruction, the E level from the major state generator is combined with the IA2 and IB2 levels from the IR decoder in NAND gate KLMN of module K12 (C1, 9) and produces a negative E · AND level. The E · AND level conditions NAND gate NPR in module J6 (C6, 26), which is triggered by timing pulse T5 and causes generation of the MB0 → AC pulse.

Pulse amplifier FDEC in module K6 which appears at terminal K6D generates the ACS1 → AC command pulse. This command pulse causes the contents of the ACCUMULATOR switches on the console to be transferred into the AC. The ACS1 → AC pulse is generated at time SP2 of a DEPOSIT or DEPOSIT NEXT key cycle. This command pulse may also be generated during the execution of an OPR instruction containing a 1 in bit 15. The MBB15(1) level conditions NAND gate JKL in module J6, and an OP 2 pulse at time T7 triggers the gate causing generation of the ACS1 → AC pulse.

The ADD OV level is generated whenever the AC overflows during an ADD instruction. This level conditions a link input gate which is strobed by timing pulse TP1 of the following cycle and sets the link to 1 if there has been an overflow. The ADD OV level appears at the junction of terminals F7F, F7L, F8J, and F8E. All four of the inverters connected to these terminals must produce a negative output level to establish an ADD OV negative level. The possibility of an overflow is detected by applying the AC0(0) status to NAND gate NPR in module F9 (B4, 9). If this bit contains a 0 after data is XOR transferred to the AC, but before the carry pulses are generated, there is the possibility of an overflow. Timing pulse T4 strobes the gate and, if bit AC0 contains a 0, the POV flip-flop is set. The buffered IR3(0) level and the POV(1) level now fulfill two of the conditions for the production of an ADD OV level. However, the states of bit MB0 and bit AC0 must now be sensed to determine whether an overflow has in fact occurred. The two NAND gates in module D7 make the comparison. If, after the carry, bit MB0 and bit AC0 both contain a 1, there has been transfer of a 1 with no overflow. Terminal D7L, therefore, remains at ground potential and prevents generation of a negative ADD OV level. Similarly, if bits MB0 and AC0 both contain a 0 after the carry, no transfer has taken place between these bits, and terminal F7F remains at ground potential. However, if bit MB0 contains a 1 and bit AC0 contains a 0 after the carry, an overflow occurs. Both NAND gates are disabled under these conditions, and a

negative output level from all four inverters generates the ADD OV level. The ADD OV level conditions a link input gate which is strobed by the following timing pulse TP1 and sets the link. A few nsec later, timing pulse T1 resets the POV flip-flop.

The OP SKP (operation skip) negative level is generated at terminal K10F and conditions a gate in the PC control that increments the contents of the PC when an OPR instruction contains any one of six possible skip microinstructions. The OP SKP level is generated and the contents of the PC incremented at time T5 if any one of the following sets of conditions is fulfilled:

a. Bit 8 is 0, bit 9 is 1, link is set.

b. Bit 8 is 0, bit 10 is 1, contents of AC are zero.

c. Bit 8 is 0, bit 11 is 1, bit AC0 is 1 (sign negative).

d. Bit 8 is 1, bit 9 is 1, link is not set.

e. Bit 8 is 1, bit 9 is 1, contents of AC are not zero.

f. Bit 8 is 1, bit 9 is 1, bit AC0 is 0 (sign positive).

The NAND gates contained in modules L8, L9, and L10 (A1, B1, 9) generate the AC = 0 and AC $\neq$ 0 levels. These NAND gates sample the contents of each individual bit of the AC and give a ground level at terminal L10V if all bits are 0.

Note that when more than one skip condition is specified in a single instruction, the combined skip condition is the inclusive OR of the individual conditions when bit 8 contains a 0.

3.3.3.2 Program Counter Register Control (8) - All of the command pulses which clear the PC, increment its contents, or cause a transfer of information into the PC from other registers are generated in the control logic circuits shown at the bottom right of engineering drawing 8. This logic element consists of six pulse amplifiers which generate the command pulses, together with diode gates and inverters which determine the conditions under which each pulse amplifier is triggered.

The pulse amplifier circuit at location F17 generates a 0 $\rightarrow$ PC command pulse which clears bits 5 through 17 of the PC. Bits 3 and 4 are used in conjunction with an extended memory and are cleared by a pulse from the Type 148 Extend Mode Control option. Any one of the following conditions clears bits 5 through 17 of the PC:

a. At time SP1 of a key cycle, after operation of the START, EXAMINE, or DEPOSIT key.

b. At time T5 of the fetch cycle of a JMP instruction, in preparation for the transfer of a new address from the MB.

c. At time T3 of the execute cycle of a JMS instruction or at time T3 of a program break cycle.

d. At time SP1 of a key cycle during a readin operation, provided that the RPT flip-flop is in the 0 state.

The pulse amplifier circuit at location F16 generates an AS1 → PC command pulse which transfers the contents of the ADDRESS switch register into the PC. Either of the following conditions generates the command pulse:

a. At time SP2 of a key cycle, after operation of the START, EXAMINE, or DEPOSIT key.

b. At time SP2 of a key cycle during a readin operation, provided that the RPT flip-flop is in the 0 state.

The pulse amplifier circuit generates an MB1 → PC command pulse which causes the contents of bits 5 through 17 of the MB to be transferred into the PC. Bits 3 and 4 receive a similar command pulse from the extend mode control. A JMP instruction generates the MB1 → PC pulse at time T6 of the fetch cycle; the information transferred is the address from which the next instruction is to be fetched.

The pulse amplifier F17 generates the MA1 → PC command pulse at time T4 of the execute cycle of a JMS instruction, or at time T4 of a program break cycle. The contents of the MA are the address at which the current program count is to be deposited; this address is 0 for the program break.

The PC+1 pulse increments the contents of the PC by 1 and is generated by two cascaded pulse amplifiers at location L16 and location J26. The second pulse amplifier introduces a delay of 20 nsec between the time at which the flip-flop outputs are sampled by the PC → MA pulse, and the time at which the contents of the PC are incremented during a fetch cycle. The gating associated with these two pulse amplifiers causes new instructions to generate the incrementing pulse during skip, jump, and special mode operations. The incrementing pulse is generated in the following circumstances:

a. At time SP2 of a read paper tape operation.

b. At time SP4, following operation of the EXAMINE or DEPOSIT key.

c. At time T1 of a fetch cycle.

d. At time T5 of the execute cycle of a SAD instruction if the contents of the AC are not 0. The E · SAD and AC $\neq$ 0 levels which condition the NAND gate in module D14 are both generated in the AC control.

e. At time T5 of the execute cycle of a JMS instruction, or at time T5 of a program break cycle. The E · JMS component of the level which conditions terminal E of module D12 is generated by the major state generator and IR decoder; the PROG · B component is generated in the interrupt control.

f. During the execute cycle of an ISZ instruction, at time T3, if a carry pulse is generated by bit MB0 of the MB, indicating that the contents of the MB are 0.

g. At time T5 of an OPR instruction microprogrammed for one of the six possible skip operations, if the conditions for the skip are fulfilled. The OP SKP (operation skip) level and the OP 1 pulse applied to terminals P and R of module F12 are both generated in the AC control.

h. At time T6 of a program break cycle after an illegal instruction is trapped, when the system is operating in the trap mode. When the TRAP FLAG flip-flop is set, a one-shot delay generates the positive TRAP pulse that is applied directly to pulse amplifier input L16F.

i. During an I/O device identification operation, when the flag of the selected device is set.

3.3.3.3 Memory Address Register Control (8) - The control circuits, shown at the top right of engineering drawing 8 generate all of the command pulses which cause a flow of information into the MA. This control element consists of two Type B602 FLIP CHIP modules, each containing two 40-nsec pulse amplifiers; a Type B113 FLIP CHIP module containing four diode gates and associated inverters; and a Type B115 FLIP CHIP module containing three diode gates and associated inverters.

The pulse amplifier circuit at location C15 generates standard negative pulses which clear the entire MA under either of the following conditions:

a. At time SP1 of a key cycle after operation of any key except the STOP key.

b. At time T7 of each computer cycle, provided that the RUN flip-flop is in the 1 state. This action prepares the MA for the insertion of a new address at time T1 of the following cycle.

Pulse amplifier C17 generates a PC1 → MA pulse which transfers information from the PC to the MA at time T1 of every fetch cycle. The address set into the MA by this action is that of the next instruction to be executed.

Another pulse amplifier C17 generates a MB → MA pulse which transfers information from bits 5 through 17 of the MB into the corresponding bits of the MA. The transfer occurs at time T1 of a defer or execute cycle, provided that the instruction below executed is not CAL (call subroutine). Either a D ground level at terminal C14D or an E ground level at terminal C14E conditions terminal C14L with a negative level. A negative $\overline{\text{CAL}}$ level derived from the MB control conditions terminal C14M. When timing pulse T1 reaches terminal C14K, the positive pulse which appears at terminal N triggers the MB1 → MA pulse amplifier.

A pulse amplifier C15 generates a 20 → MA pulse which sets octal 20 into the MA during the defer or execute cycle of a CAL instruction. A negative D or E level and a negative CAL level derived from the MB control conditions NAND gate RSTU of module C14. When timing pulse T1 reaches terminal R, the positive pulse appearing at terminal U triggers the 20 → MA pulse amplifier.

3.3.3.4 Memory Buffer Register Control (8) - The logic circuits, shown at the left of engineering drawing 8, generate all the command pulses which clear the MB, increment its contents, and cause or inhibit a transfer of information into the MB. Four pulse amplifiers contained in two Type B602 FLIP CHIP modules and one Type B620 Pulse Amplfier generate command pulses. A Type B684 Bus Driver provides negative or ground levels, which condition or inhibit the gates connecting the MB to the memory sense amplifiers. Diode gates and inverters combine various levels and timing pulses to select the conditions under which each command pulse is generated.

The 0 → MB command pulse generated by the pulse amplifier circuit RNPM at location F1 clears the entire MB register. The BGN pulse of a key cycle triggers this pulse amplifier at time T2 of every computer cycle, and at time T7 of an execute cycle initiated by a readin operation.

The Type B684 Bus Driver at location C10 produces a negative $\overline{\text{MB STB INH}}$ (not MB strobe inhibit) level continuously, thereby permitting the logic 1 pulses generated by core memory sense amplifiers to set the corresponding MB flip-flops during the read operation in every cycle. During certain operations, however, the contents of a memory cell are not transferred into the MB. For these operations, a ground MB STB INH level inhibits the gates between the sense amplifiers and the MB. Any one of the following conditions causes generation of the MB STB INH level:

a. During a program break cycle, the negative PROG · B level generated by the interrupt control is applied to terminal T of diode gate module K21 and is inverted.

b. A high-speed I/O device requesting a break cycle to deposit information in memory generates a negative DATA-IN level, which conditions terminal K21K. When the data break is granted, the negative DATA · B level produced by the interrupt control conditions K21J and causes the NAND gate to produce a ground level at the input of the bus driver.

c. During the execute cycle of a JMS or DZM instruction, the E level from the major state generator conditions terminal K21E; and the IA0 level produced by the IR decoder conditions terminal K21D. The NAND gate then produces a ground level output which is applied to the bus driver.

The MB+1 command pulse increments the contents of the MB by 1 and is generated by two cascaded pulse amplifiers: FDEC of module E1 and EHD of module J26. Any one of the following conditions triggers these pulse amplifiers:

a. Time T3 of a defer cycle, when the contents of the MA are one of the auto-indexing locations 10 through 17. All of these locations only are defined by a 0 in MA bits 5 through 13 and a 1 bit 14. The MA5-13(0) and MA14(1) levels are combined in module F6 with the D level from the major state generator and condition input terminal P of a NAND gate in module F2. When timing pulse T3 is applied to terminal F2N, the gate is triggered, and its positive output pulse causes the pulse amplifiers to generate the +1 → MB pulse.

b. When a real-time clock is in use and is enabled by the program, the CLOCK · B level produced by the interrupt control when a clock break is granted conditions the NAND gate in module F2. Timing pulse T3 triggers the gate and causes generation of the +1 → MB pulse.

c. During the execute cycle of an ISZ instruction, the E level from the major state generator and the IA2 and IB1 levels produced by the IR decoder are NAND combined in module F5. The output of the gate is inverted and conditions NAND gate in module F2. When timing pulse T3 is applied to terminal F2D, the gate is triggered and causes generation of the +1 → MB pulse.

Pulse amplifier circuit RNPM of module E1 generates the AC1 → MB command pulse which causes the contents of the AC to be transferred into the MB. This command is generated only during the execute cycle of a DAC instruction. The E level from the major state generator is NAND combined in module F5 with the IA0 and IB1 levels produced by the IB decoder. The output of the gate is inverted and conditions NAND gate TUV in module F2. When timing pulse T3 is applied to terminal T, the gate is triggered and causes generation of the AC1 → MB pulse.

The PC1 → MB command pulse is generated by pulse amplifier circuit FDEC in module F1 and causes the contents of the PC to be transferred into the MB. Any one of the following conditions generates this command:

a. During a read paper tape operation, the RPT(1) level conditions NAND gate DEF in module F9. Timing pulse SP4 triggers the gate, and the positive pulse which appears at terminal F triggers the pulse amplifier.

b. During an examine or deposit operation, the EX+EXN+DP+DPN level generated by the key circuits conditions NAND gate JKL in module F3. Timing pulse SP3 of the key cycle triggers the gate and causes generation of the PC1 → MB pulse.

c. During a program break cycle or the execute cycle of a JMS instruction, the E · JMS+PROG · B level conditions NAND gate DEF of module F3. Timing pulse T3 triggers the gate and causes generation of the PC1 → MB pulse.

3.4 CORE MEMORY

Data and instruction storage and retrieval are performed in the PDP-7 by the core memory. The standard PDP-7 is equipped with a DEC Type 149A Memory Module which can store 4096 18-bit words and which requires a 12-bit address. The addition of a DEC Type 147 Core Memory Module expands the memory capacity of the Type 149A Memory Module of the standard PDP-7 to 8192 words. No auxiliary equipment is required since the existing 15-bit memory address register (MA) provides the extra address bit required for selecting addresses in either 4K memory array. Memory capacity can be further expanded by increments of 4096 or 8192 words to a maximum of 32,768 words. Expansion beyond 8K requires the use of a DEC Type 148 Memory Extension Control and the remaining two bits of the MA supplied within Type 148. All information enters and leaves core memory via an input/output register designated the memory buffer register (MB). This manual describes the operation of the 8K memory; the basic principles and methods of access to this memory are equally applicable to larger or smaller capacities. For information on methods of accessing extended memories, refer to the maintenance manual for the Type 148 Memory Extension Control.

3.4.1 Memory Organization

Each 4K core memory module used in the PDP-7 is a simple, coincident-current, ferrite core array assembled from core planes 64 cores wide by 64 cores deep. Each module is operated by read, write, and inhibit currents and gating circuits. Figure 3-3 shows the interrelationship of the elements which constitute the core memory system. The MA and MB are located in the central processor (CP). Timing

signals which control memory functions are derived from the CP timing signal generator in order to synchronize memory operations with CP operations. The memory cycles perform a read operation during time states T2 and T3 and a write operation during time states T5 and T6. This permits random bidirectional access to any memory cell within one 1.75-μsec computer cycle. Both reading and writing operations are performed during each cycle, since reading from a memory cell destroys the contents. Thus, if the information is not to be lost, it must immediately be rewritten into the same cell from the MB. The only exceptions to this rule occur during a data break in which the direction of transfer is into the computer core memory and during the execution of DAC, read/modify/write cycle of ISZ, CLK, auto index, JMS, or DZN instructions.

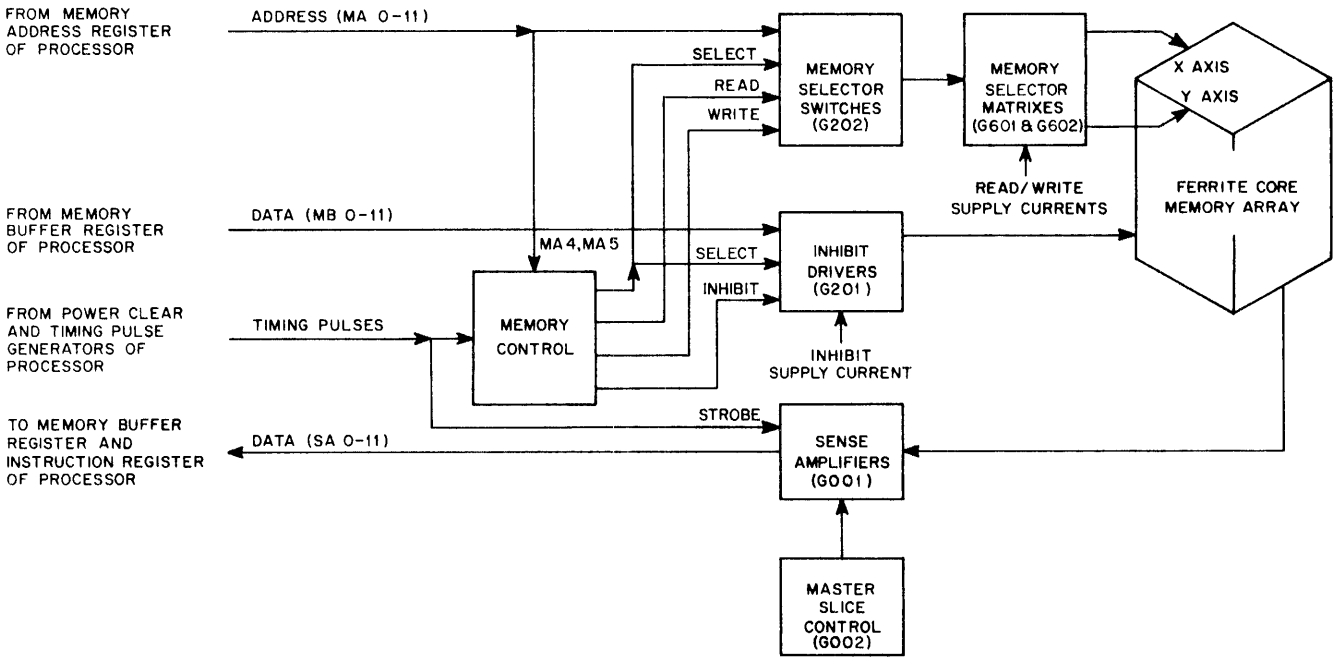


Figure 3-3 Core Memory System Block Diagram

3.4.2 Circuit Operations

3.4.2.1 Ferrite-Core Memory Array - The standard memory array consists of 18 planes, each having 4096 ferrite cores arranged in a 64 by 64 square. Each core can assume one of two stable magnetic states corresponding to binary 1 and binary 0. Four windings traverse each core. An X read/write winding passes through all the cores in one horizontal row; a Y read/write winding passes through all the

cores in one vertical row; the sense and inhibit windings each pass through all the cores in the plane. Figure 3-4 shows an example of this winding for a 4 by 4 core plane. In figure 3-4, passing a current from right to left (write direction) of the diagram through the X2 winding produces a magnetic field that tends to change all the cores in that row from the 0 to the 1 state. Passing a current from bottom to top of the diagram through the Y3 winding produces a similar effect on the cores in that row. Neither the X current nor the Y current is, by itself, strong enough to change the state of any core. However, if both X2 and Y3 currents are turned on, the magnetic fields caused by the two currents are mutually reinforcing in one core through which both windings pass. The combined strength of both fields causes this, and only this, core (in each plane) to change state to the 1 condition. In the PDP-7 system, an array consists of 18 planes, with all the corresponding address windings connected in common so that each plane can be considered equivalent to one bit of a storage cell. Thus, in the previous example, the core located at coordinates X2Y3 on each plane will change to the 1 condition unless an inhibit current prevents it from doing so.

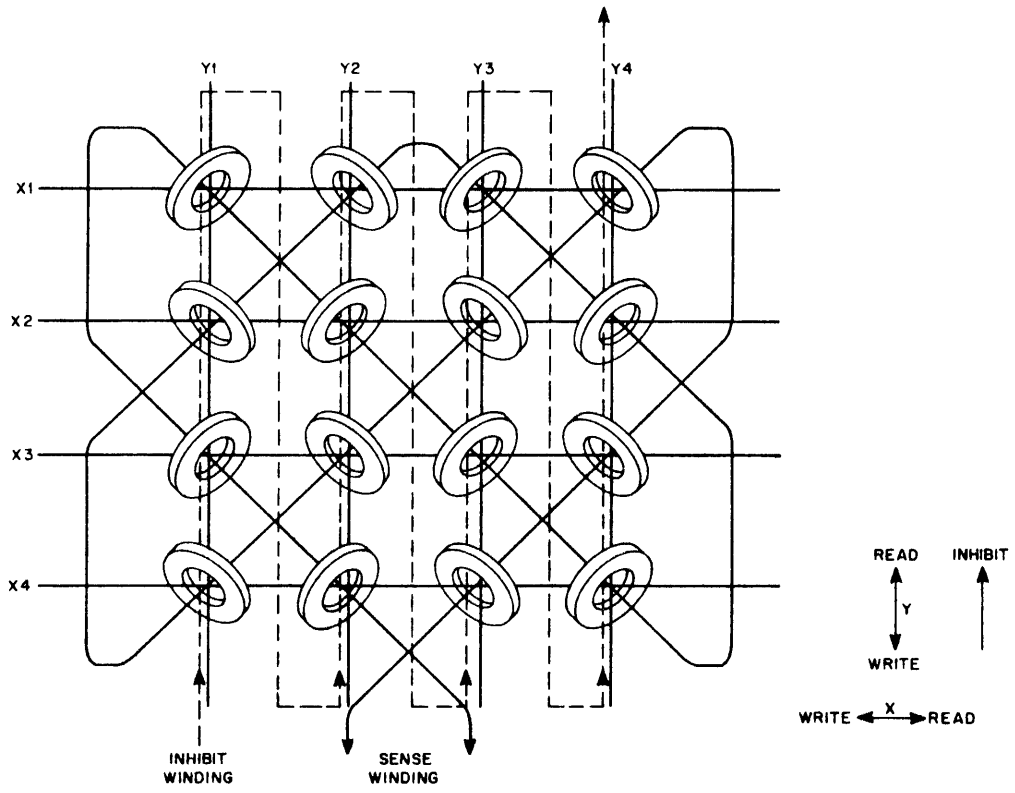


Figure 3-4 Simple Core Memory Plane Showing Read/Write, Sense, and Inhibit Windings

If the storage cell consisting of X2Y3 cores is to contain 0s as well as 1s, the cores in the planes which correspond to 0 bits must be prevented from changing state when the writing currents are turned on. This is accomplished by passing a current through the inhibit windings of those planes. The magnetic field due to the inhibit current has a direction and amplitude which partially cancels the fields due to the writing currents. Thus, even though both X and Y writing currents are present in all the X2Y3 cores, those cores in planes where an inhibit is also present remain in the 0 condition. After setting or resetting cores, all of the read/write and inhibit currents are turned off without affecting the state of any core.

To read the information stored in the X2Y3 cell, currents must be passed through all the X2 and Y3 windings in the opposite direction, thereby tending to change all the X2Y3 cores to the 0 condition. Cores X2Y2 of all planes which were inhibited during writing, and are thus already in the 0 state, induct only a very small signal into the sense windings. However, X2Y3 read currents are turned on. The resulting flux change induces a relatively large signal into the associated sense windings. After amplification, these binary 1 signals complete the information transfer by setting the corresponding MB flip-flops.

3.4.2.2 Memory Selectors Type G202 and Memory Selector Matrixes Types G601 and G602 - The memory selectors decode the information contained in the MA and perform memory cell selection; the memory matrixes, controlled by the memory selectors, route read and write current pulses to the selected memory cell. In each memory array, address bits MA6 through MA11 select read and write lines in the matrix of the Y axis; bits MA12 through MA18 select read and write lines in the matrix of the X axis. Drawing E-149-0-9 shows the circuits for Y axis selection. Note that the four Memory Selector Type G202 modules, known as drive selectors, shown at the left of the diagram, decode address bits MA6 through MA8. The four G202 modules shown at the bottom of the diagram, known as ground selectors, decode address bits MA9 through MA11. The selector modules provide pulses to open gates in the Memory Selector Matrix Type G601 and G602 modules. A similar arrangement of memory selectors and memory selector matrix modules provides selection of read/write lines on the X axis, as shown in drawing E-149-0-98. Drawing RS-B-G202 contains a schematic diagram of a memory selector. Drawings RS-D-G601 and RS-D-G602 contain schematic diagrams of the matrixes.

The following discussion of the core selection process is based on the simplified schematic diagram of figure 3-5. This diagram shows the logic switching circuits involved in the generation of read and write currents for cell 46 on the Y axis. When cell Y46 is to be read, the address set into the MA contains MA6(1), MA7(0), MA8(0), MA10(1), and MA11(0) which are applied as negative assertion levels to the selector module. Negated ground levels corresponding to $\overline{\text{MA8(1)}}$ and $\overline{\text{MA11(1)}}$ are also applied to the selector modules. The $\overline{\text{MA6(1)}}$ and $\overline{\text{MA7(0)}}$ negative levels enable transistor switches Q4 and Q5, respectively, of the drive selector module at location A10; similarly, the MA9(1) and MA10(1)

levels enable transistor switches Q4 and Q5 of the ground selector module at location A13. The MA8(0) and MA11(0) levels are both negative, thereby enabling transistor switch Q7 in both modules. A negated ground level corresponding to MA8(1) and MA11(1) disables transistor switch Q2 in each module. These levels are established as soon as the cell address is loaded into the MA during time state T1 of the computer cycle.

At time T2, timing pulse TP2 sets the READ 2 flip-flops (figure 3-6). The setting of the READ 1 flip-flop, in combination with the state of the field select bits, MA4 and MA5, causes a SEL 1 · READ 1 level to be applied to the G202 Pulser Selector, which in turn applies a pulse to the read pulser, thereby connecting read drive bus 4 to the positive supply. Simultaneously, the READ 2(1) level enables transistor switch Q4 in both drive and ground selectors. The surge of current through the transistors causes pulses to be generated which open pulse gates PG1 and PG4. A read half-select current then flows from the read/write memory current supply through the read pulser, pulse gate PG1, diode D1, the cores of cell Y46, diode D3, and pulse gate PG4 to the read/write common negative line. This half-select read current is factory adjusted to approximately 330 ma. At time T3, the READ flip-flops are both cleared in preparation for a write operation.

At time T4, timing pulse TP4 sets the WRITE 1 and WRITE 2 flip-flops, thereby enabling the write pulser and transistor switch Q_8 in the drive and ground selector modules. The resulting pulses connect write drive bus 4 to the positive read/write current supply and opens pulse gates PG2 and PG3. A write half-select current then flows from the supply, through pulse gate PG2, diode D4, the drive lines of the cores of cell Y46 (in the opposite direction to the read pulse), diode D2, and pulse gate PG3 to the read/write common negative line.

3.4.2.3 Inhibit Drivers Type G201 - The PDP-7 memory is wired for 19 Inhibit Driver modules Type G201. Each of these modules energizes the inhibit winding of one memory plane. Note, however, that the 19th plane is not used in the PDP-7 system unless the Type 176 Parity Checking option is in use, in which case a 19th plane and an inhibit driver module are added and used for a parity bit. A schematic diagram of an inhibit driver is shown in drawing RS-B-G201, and the connection of the inhibit drivers in the memory system is shown in engineering logic diagram E-149-0-45. Figure 3-7 shows the internal logic circuits of an inhibit driver. A negative INH B level is applied to the module at terminals F and J and is NAND combined with the negative 0 level of the associated MB bit in transistor switches Q2 and Q5. The combined signal output of transistor switch Q5 enables pulse gate 1, which provides the principal on/off switching for the inhibit current. The INH B · MB(0) signal and the appropriate array SEL signal are NAND combined in transistor gate Q2 or Q3. If a negative SEL 0 level is present, transistor Q3 conducts and enables pulse gate 2, thereby routing the inhibit current into the inhibit winding associated with bit X of memory array 0. If a negative SEL 1 level is applied to transistor gate Q4, pulse gate 3 is enabled and routes the inhibit current into the corresponding bit inhibit winding of memory

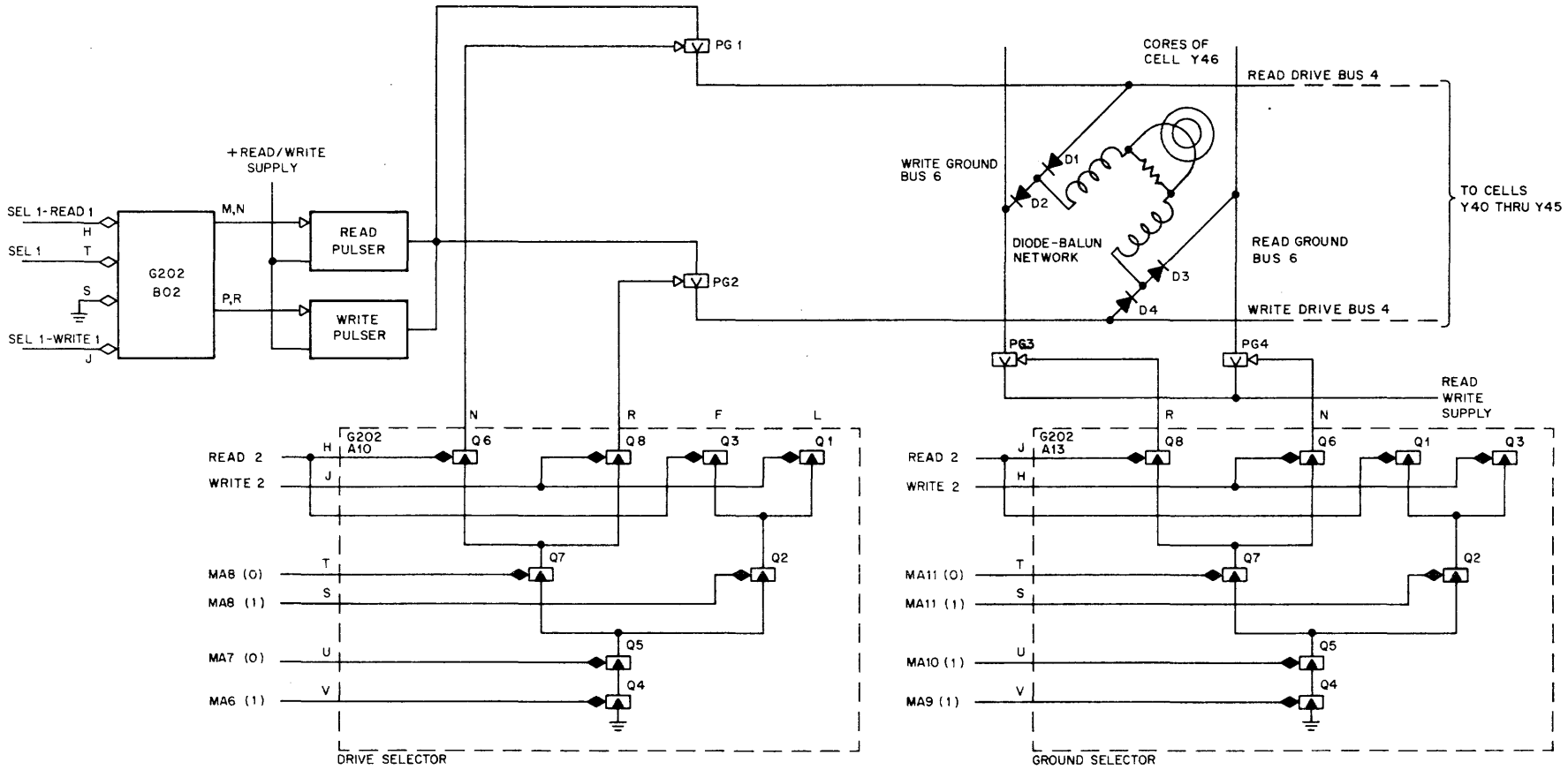


Figure 3-5 Typical Core Selection Circuit and Drive Current Path

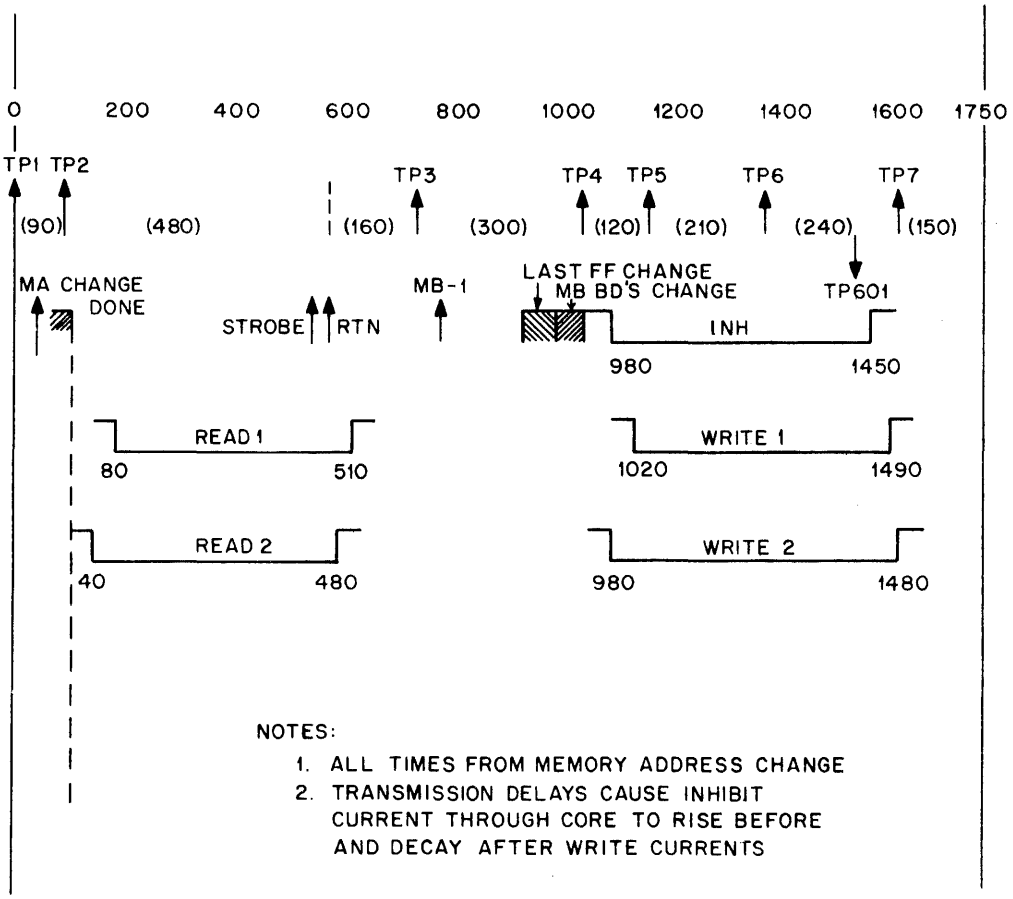


Figure 3-6 Memory Control Timing

array 1. The memory control logic ensures that SEL 0 and SEL 1 levels can never be applied simultaneously. Inhibit current is applied to the inhibit winding of the cores through a balun which balances the winding with respect to ground, thereby minimizing the effects of stray capacitance and permitting increased optional speeds in memory. Each Type G201 Inhibit Driver can sustain a current of 350 ma for 500 nsec; however, in the PDP-7 system, the inhibit current is normally set at approximately 290 ma.

3.4.2.4 Sense Amplifiers Type G001 and Master Slice Control Type G002 - The PDP-7 memory contains 19 Sense Amplifier modules Type G001 and one Master Slice Control module Type G002. Eighteen of the sense amplifiers supply a standard negative pulse to the MB when an associated core changes from the 1 state to the 0 state during a read operation. The 19th sense amplifier provides a parity bit when the Type 176 Parity Checking option is in use. The master slice control supplies all the sense amplifiers with closely controlled reference voltages for use in clamping and comparator stages. Drawings

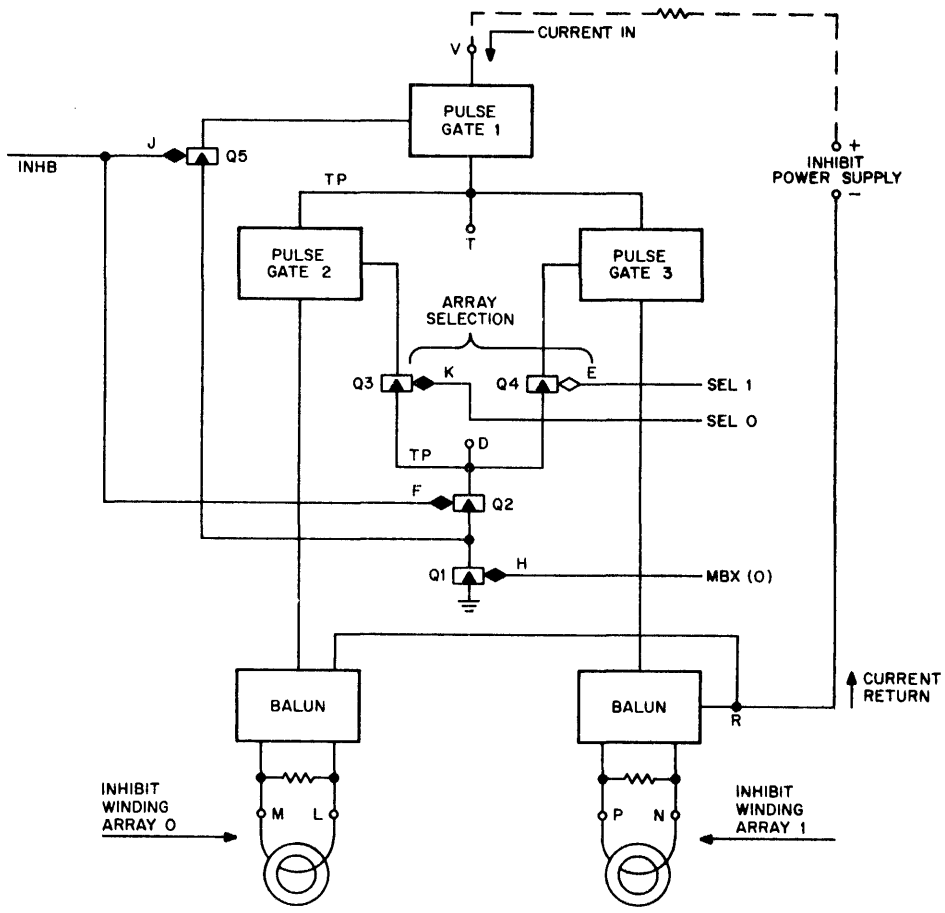


Figure 3-7 Inhibit Logic for One Memory Cell

RS-B-G001 and RS-B-G002 contain schematic diagrams of the sense amplifier and the master slice control, respectively. The connection of these modules in the memory system is shown in drawing BS-E-149-0-45.

Each sense amplifier contains a 2-stage dc preamplifier, a rectifying slicer, an output gate, and a pulse amplifier. The first stage of the dc preamplifier has two separate gated difference amplifiers, which share a common push-pull output stage. One input difference amplifier accepts a pulse input from the sense winding of the associated plane in memory array 0, together with a SEL 0 ground level which gates on the difference amplifier. The other input difference amplifier accepts a pulse from the corresponding plane in memory array 1 and a SEL 1 enabling level. The memory control logic provides the enabling levels which ensure maximum stability. The slicer suppresses nodes induced into the sense winding of a memory plane by the read/write current pulses. Therefore, only the much larger signal produced by a core changing state can produce an output from the sense amplifier.

In order to obtain an output pulse of the correct shape and duration, a strobe pulse is applied to the output gate of the sense amplifier. The strobe pulse is obtained by combining timing pulse TP2 of the computer timing chain with a field selection signal, applying the resulting pulse to a delay network, and reshaping the delayed pulse in a pulse amplifier.

The strobe pulse is precisely timed with respect to the read current pulse, so that sensing occurs at the instant when the signal induced into the sense winding reaches maximum peak amplitude (figure 3-6). If a core changes state, the slicer enables the output gate, and the strobe pulse causes the gate to produce a 40-nsec output pulse. This pulse is reshaped in the pulse amplifier and appears at the output terminal of the module as a standard negative pulse which sets an MB flip-flop.

The master slice control module contains three reference voltage diode networks, each with an associated emitter follower output voltage control. The adjustment range of the first stage clamp potential is from 5.0 to 6.5v; that of the second stage clamp potential is from 11.5 to 12.4v; and that of the slice level is from 5.0 to 10.0v. The first and second stage clamp levels are factory preset at 6.5v and 11.4v, respectively, under a 50-ma load. The slice level is normally preset to 6.8v and may be adjusted so that the sense amplifier gives symmetrical deviations when the sense amplifier +10v supply is varied to the upper and lower marginal levels.

3.4.2.5 Memory Control - The memory control logic generates signals which perform memory array selection and initiate the generation of read, write, and inhibit currents at the appropriate times in the computer cycle. The logic diagram of the memory control is contained in drawing D-KA77A0-10, and all references in the following discussion of the memory control are to this diagram unless otherwise stated.

NAND gates in modules E21 and E22 decode address bits MA5(0) and MA5(1) producing SEL 0 SEL 1, SEL 2, and SEL 3 control signals. Each of these signals enables the sense amplifier gates associated with a particular 4K memory array. When memory capacity is limited to 8K, bit MA4 is always 0, and bit MA5 selects one of the arrays in the 8K field designated. At time T2 of the computer cycle, timing pulse TP2 sets the READ 1 and READ 2 flip-flops. The READ 1 ground level output is combined with the MA5(0) or MA5(1) level to produce a SEL · READ(1) B level which enables the read current pulser in the address selection circuits. The negative READ 2(1) level is applied to the drive selectors and ground selectors. At time T3, the STROBE 0, 1 pulse clears the READ 2 flip-flop first in order to disable the read/write current pulsers; 30 nsec later, the STROBE RTN pulse clears the READ 1 flip-flop to disable all the read gates in the drive and ground selectors. The setting of the WRITE flip-flops results in similar actions, except that the WRITE 2 flip-flop opens the write gates in the memory selectors, thereby reversing the direction of the current pulse through the memory cores.

The memory control logic includes bus drivers which provide adequate current to drive the memory selectors and to gate the inhibit drivers. The NAND gates in module E29 combine address bit MA4 with timing pulse TP2 for the generation of a separate strobe pulse for each of two 8K memory fields. When memory capacity is limited to 8K, the TP2 · SEL 0, 1 pulse is used. The resulting strobe pulse is applied to both 4K arrays of the 8K memory field.

3.4.2.6 Memory Current Sources - A Type 739 Power Supply is used in conjunction with the Core Memory Type 149B. The Type 739 unit contains two independent, floating power supplies. One supply provides read/write current, and the other provides inhibit current for a complete PDP-7 system, regardless of the capacity of the memory. A Type 728 Power Supply provides +10v and −15v to energize the memory logic. Both the 728 and 739 units are located at the rear of equipment bay 1, behind the memory. Circuit schematic diagrams for the 739 are shown in engineering drawings RS-C-739B, RS-B-W505, and RS-G-800. Engineering drawing RS-B-728 shows the circuit schematic for the Type 728 Power Supply.

3.5 INTERFACE AND INPUT/OUTPUT

All information transfers between the CP and I/O equipment (other than devices which use the data break facility) take place under program control by way of the interface equipment and the accumulator register. Selection of an I/O device and generation of control pulses takes place in the interface logic. Gating circuits to control information flow are located at the input of the receiving register. The interface information transfer logic consists of four elements:

a. A device selector which decodes the IOT instruction to be executed, addresses the appropriate I/O device, and generates up to three IOT command pulses for control purposes.

b. An information collector which gates incoming information into the accumulator register.

c. An information distributor, consisting of bus drivers capable of driving an output system through which information is transferred from the accumulator register to I/O devices.

d. The CLK, FLG, SKP and PWR CLR logic which controls the sequence of programmed operation.

The interface is packaged in bay 3; rows A through J. The drawing set number for the interface is KA-71A-0 (1 through 14). This drawing set also includes the control logic for the I/O equipment supplied with the standard PDP-7.

3.5.1 Device Selector (KA-71A-5)

The device selector (DS) logic generates IOT pulses to control the I/O equipment and to determine the data transfer sequence between the I/O device and peripheral equipment. For standard IOTs, when MB 6, 7, and 8 are 0, the IOT 0xen level developed at the B117 NAND Gate (D5:5) enables the R151 Standard IOT Decoder. The R151 Decoder decodes MB bits 9 through 11 to enable one of the eight standard device selectors. Each standard device selector consists of a B115 Gate, an R107 Gate, and an R603 Pulse Amplifier. See table 4 of the PDP-7 Interface and Installation Manual F-78A for device selector channel assignments. See drawing KA-71A-6 for optional device selector coding.

3.5.2 Information Collector (KA-71A-4)

The IC consists of 18 R141 Multiple Diode Gate Modules. The IC reads data or status information into the AC from various devices. Seven IC channels or levels are available in the basic machines. Each of these channels is wired to a signal cable connector corresponding to an upper half (bits 0-8) and a lower half (bits 9-17) of the AC for optional equipment, or is wired directly to controls for the standard PDP-7 I/O equipment. On the basic machine, the paper-tape reader occupies one complete channel, the Teletype occupies the lower half of a channel, and the status register occupies (nominally) one channel. If no card reader, card punch, or line printer is connected to the system, the lower half of the status register channel may be used for other purposes. Thus, in the basic machine, the equivalent of five free channels is available for additional IC inputs. Channel availability of the IC is specified as follows:

Level	Use
1	All 18 connections employed for RB of the tape reader.
2	First 9 connections employed for status signals of IORS instruction (IOT 0314), and last 6 connections are assigned to the step counter (SC) of the Type 177 EAE option, when present.
3-5	All 18 connections open and assignable.
6	First 10 connections are open, and last 8 connections are assigned to Teletype unit.
7	First 12 connections open and assignable.

Each level or channel of the IC consists of one 2-input negative AND gate for each of the 18 possible bits of an input word. The two inputs are usually supplied by a data signal and an IOT pulse which is common to each bit of the input word. Outputs from the seven channels for each bit are NOR combined to set the appropriate accumulator flip-flop. One bit for each of the seven channels is provided by a Type R141 Diode Gate module; the entire IC is constructed of 18 of these modules.

When designing a PDP-7 system, it is necessary to consider the number of IC channels required by peripheral equipment. If more than seven channels are required, the IC must be expanded to accommodate the additional information. Expansion requires a Type 175 Information Collector Expander consisting of 18 Type R141 Diode Gate modules, 6 Type W640 Pulse Amplifier modules, and the appropriate mounting panel and hardware. The Type 175 option connects into the standard IC through two signal cable connectors reserved for this purpose, and adds seven additional information channels.

3.5.3 Information Distributor

The information distributor of the basic PDP-7 system consists of 16 Type W021 Cable Connectors to distribute the bus driver output signals. Negative logic 1 assertion levels from the AC appear as ground logic 1 assertion levels on the distribution buses. The information distribution can be expanded almost indefinitely by adding W021 Connectors, with additional bus drivers if the maximum load on the standard drivers is likely to be exceeded.

3.5.4 MB Bus Drivers

The 1 levels of the MB flip-flops are available for distribution within the CP and to external devices connected to the data channel. Nine Type B684 FLIP CHIP Bus Driver modules are used. Each module contains two bus drivers, and each bus driver can supply up to 40 ma of load.

3.5.5 Control Signals

3.5.5.1 Power Clear Output Signals - The PWR CLR POS and PWR CLR NEG pulses generate in the I/O package during the first 5-sec interval following setting of the POWER switch to the on position. These pulses initialize and clear processor registers and control during the power turn-on period, and are available to perform similar functions in external equipment. The PWR CLR POS signal is a 375-kc 100-nsec positive pulse generated in the Type R401 Clock module at location C15. The PWR CLR NEG signal is a 400-nsec negative pulse produced in a pulse amplifier of the Type W640 module at location C13 that is triggered by the PWR CLR POS pulses.

3.5.5.2 Begin Buffered Output Signal - The BGN (B) signal is supplied to external equipment through a connection in the I/O package interface. This signal is a 400-nsec, −3v pulse generated by a W640

Pulse Amplifier at location C13 of the I/O package during timing pulse SP1 · CONTINUE NOT. In I/O equipment, the signal clears registers and resets control flip-flops to initial conditions when the START key on the PDP-7 operator console is operated.

3.5.5.3 Run Output Signal - The 1 output of the RUN flip-flop is supplied to external equipment through the interface circuits. This RUN(1) signal is a −3v when the computer is performing instructions and is at ground potential when the program is halted. Magnetic tape and DECtape equipment use this signal to stop transport motion when the PDP-7 halts, preventing the tape from running off the end of the reel.

3.5.5.4 Slow Cycle Request Input Signal - The device selector supplies the SLOW CYCLE REQUEST ground level signal to request that all IOT instructions which address a specific device be executed in a computer slow cycle. This signal is added at the time a slow I/O device is added to the computer system. IOT instructions for the device are decoded in a Type W103 Device Selector module. The ground level output at terminal BD when the device is selected requests the slow cycle by connection to the input of a Type B171 Diode Gate module. This latter module is used as a ground level NOR gate for all such request signals, and a negative output on terminal D of this module is applied to the processor timing circuits. The Type B171 module which receives the SLOW CYCLE REQUEST signals from various devices is located at E14 of the I/O package.

3.5.5.5 Program Interrupt Request Input Signal - The flag of an external device can request a program interrupt. When the device requires servicing, the condition of the flag, connected to the Type B124 Inverter module in location D27 of the I/O package, can request a program break. (The flag of the external device should also be connected to the I/O skip facility so that the interrupt program can sense the IOT 01 pulse to determine the device requesting the program break.) The PROGRAM INTERRUPT signal level is the NOR of requests from up to nine devices that require programmed attention. The program interrupt facility can be expanded to accommodate requests from nine additional devices by inserting another Type B124 module in location D28 of the I/O package. When the program break is entered, a subroutine is initiated to determine which device, of many, is to be serviced, and then to perform the appropriate service operation (usually by supplying or receiving data under program control).

3.5.5.6 Data Break Request Input Signal - A high-speed I/O device may originate a data break request by placing a −3v DATA RQ level on the request line connecting the device to the computer. In the interrupt control, the DATA RQ level is synchronized with delayed timing pulse T5 (T5-DLY) of the

current computer cycle, and sets the DATA SYNC flip-flop to 1. This causes a BK RQ level to be transmitted to the major state generator. Completion of the current instruction permits the major state generator to enter a break state, producing a (B) level. This (B) level combines with the DATA SYNC level to produce a negative DATA · B level.

An external device connected to the data break facility of the computer supplies a DATA RQ level, a 15-bit core memory address for the transfer, a signal indicating the direction of the transfer as into or out of the computer core memory, and input or output connections to the MB for 18 data bits. The DATA RQ level is sent to the computer at the time the data is ready for a transfer into the PDP-7 or when the data register in the external device is ready to receive information from the PDP-7. This request level must be −3v for assertion, meaning a request for a data break, and drives a transistor base requiring 2 ma of input current.

3.5.5.7 Transfer Direction Input Signal - The computer receives this signal, specifying the direction of data transfer for a data break, from the requesting device. Transfer direction is referenced to the computer core memory, not to the device. This signal is a −3v level when the transfer direction is in, or is ground for an out transfer. A 3-input NAND diode gate for negative levels receives this signal at terminal N18F. The gate also receives the internally generated DATA · B level and T3 pulse to cause generation of the DATA ACC pulse which strobes the DI lines into the MB.

3.5.5.8 Data Address Input Signal - During an ADDR ACC pulse of a break cycle, connections made at the DA level input of a NOR gate in each module of the MA transfer the data address given by an I/O device to the MA.

3.5.5.9 Address Accepted Output Signal - At time T1 of the break cycle, the DATA · B level NAND combines with timing pulse T1 to produce an ADDR ACC pulse (called DATA ADDR → MA pulse in early systems). This pulse transfers the memory address in the address register of the I/O device into the processor MA. This pulse also acknowledges to the external device that its address has been accepted.

3.5.5.10 Data Information Input Signals - The 18 DI lines establish the data to be transferred into the MB from an external device during a data break in which the direction of transfer is into the PDP-7. The DATA ACC pulse transfers the DI signal levels, presented to 2-input negative NAND diode gates at the binary 1 input of the MB, into the MB. This information in the MB is then written into core memory during a normal write operation. The DI signals are −3v to designate a binary 1 or ground potential to specify a binary 0, and should be available at the time the break request is made.

3.5.5.11 Data Accepted Output Signal - During time T3 of a data break cycle, when the external device requests a transfer into the PDP-7, the DATA · B level causes a negative DATA ACC pulse (called DATA INFO → MB in early systems) to be generated. This pulse strobes the data input gates of the MB to transfer a data word from an external device into the MB. This pulse is also an output for device synchronization. Starting at time T5 the normal write operation writes information in the MB into core memory.

3.5.5.12 Data Ready Output Signal - During T3 of a data break cycle in which the transfer direction is out, the DATA · B level causes a negative DATA RDY (in early systems called MB INFO → OUT) pulse to be generated. This pulse may strobe MBB information into the external device buffer; for this purpose the signal may be delayed within the device to strobe the data into the buffer after an appropriate setup time. Note that the transfer must occur prior to T2 of the next computer cycle.

3.5.5.13 Data Information Output Signals - Data break transfer from core memory to an I/O device is made through the MB, whose output is buffered for this purpose by 18 Type B684 Bus Drivers. Each bus driver is capable of driving a 40-ma load. The MBB output terminals are in the I/O package.

3.6 INPUT/OUTPUT

Peripheral equipment may either be asynchronous with no timed transfer rates or synchronous with a timed transfer rate. Devices such as the CRT displays, teleprinter-keyboard, and the line printer can be operated at any speed up to a maximum without loss of efficiency. These asynchronous devices are continuously on and ready to accept data; they do not turn themselves off between transfers. Devices such as magnetic tape, DECtape, the serial drum, and card equipment are timed-transfer devices and must operate at or very near their maximum speeds to be efficient.

Some of the timed-transfer devices can operate independently of the central processor after they have been set in operation by transferring a continuous block of data words through the PDP-7 data interrupt facility. Once the program has supplied information about the location and size of the block of data to be transferred, the device itself actually performs the transfer. The data interrupt facility logic is described in Processor Logic section of this chapter.

Separate parallel buffers are provided on each input/output device attached to the basic PDP-7. The high-speed perforated Tape Reader Control Type 444B contains an 18-bit buffer and binary word assembler. The high-speed perforated Tape Punch Type 75D, and the teleprinter and the keyboard of the Teletype and Control Type 649 each contain separate 8-bit buffers. These devices are described in this chapter, and the buffers are located in bay 3 as part of the KA-71A interface package.

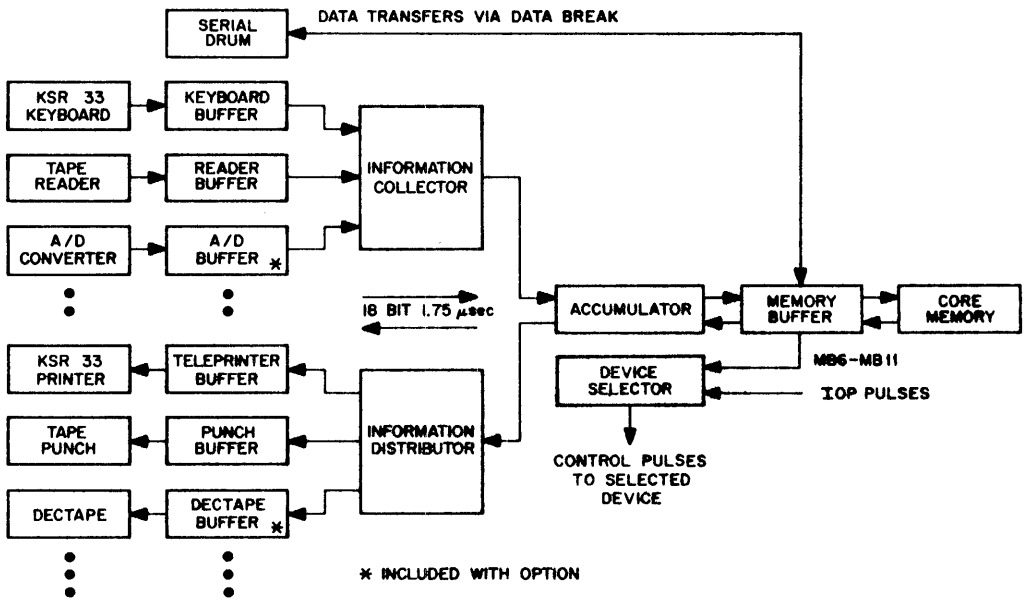


Figure 3-8 Input/Output Information Flow

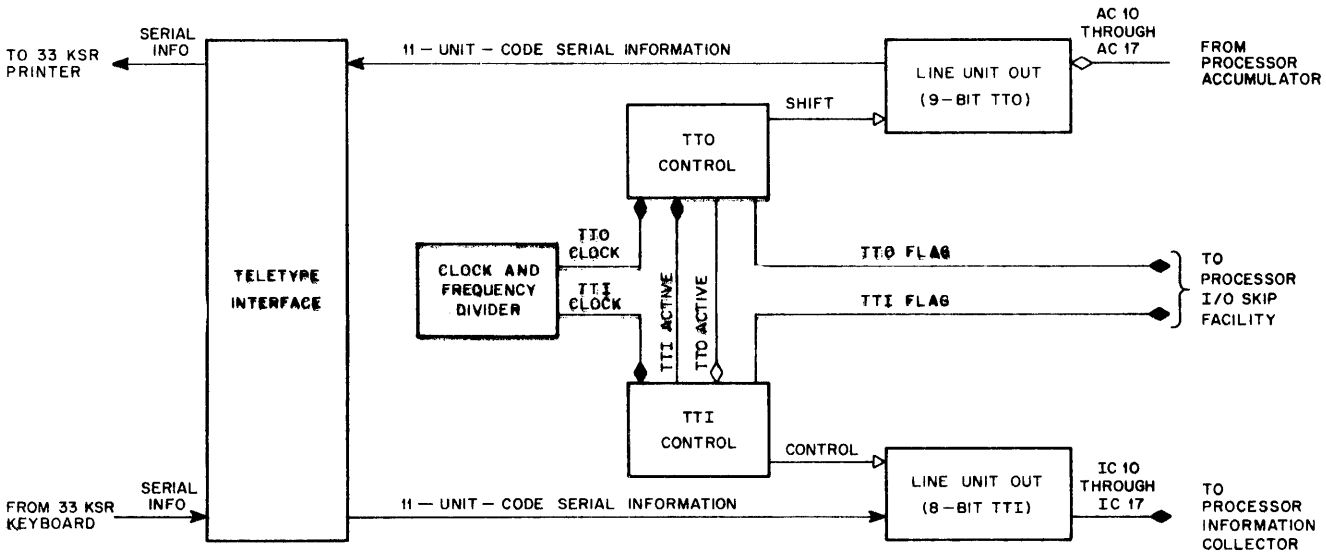


Figure 3-9 Block Diagram of Keyboard/Printer Control Type 649

Separate parallel buffers are also incorporated as part of DEC standard I/O peripheral equipment options. Information is transferred between the accumulator and a device buffer during the execution time of a single-cycle IOT instruction. Because the maximum time the accumulator is associated with any one external buffer is 1.75 μsec, many standard I/O devices can operate simultaneously under control of the PDP-7. Figure 3-8 shows the data path between device buffers and the AC through the information collector or information distributor.

3.6.1 Teletype Model 33 Automatic Send/Receive Set

The Teletype unit supplied as standard equipment with a PDP-7 serves as a keyboard input and page printer output, and as a perforated-tape reader input and a tape-punch output device. This unit is a standard Model 33 Automatic Send/Receive Set (ASR) as described in Teletype Corporation bulletins 273B and 1184B. For operation with the PDP-7, this unit is modified as follows:

a. The WRU (who are you) pawl is removed. This pawl is used only when several Teletypes connect in a communication system so that a unit receiving a message sends a "who are you" message to the transmitting unit which automatically produces the "here is" identification code and supplies it to the receiving station. In the computer system this pawl is removed to prevent insertion of the "here is" code into data supplied to the computer from the Teletype unit.

b. Signal cables connect to a terminal block within the stand, a relay is added, and connections are made to the tapereader advance magnet. These connections enable tape motion while the control assembles a character, and disable the magnet when the keyboard flag is a 1, indicating that the assembled character is ready for transfer to the computer.

This modification takes only a few minutes and does not permanently limit any normal use of the 33 ASR.

3.6.1.1 Teleprinter Control KA71A-0-9 - The control assembles or disassembles serial information for the Teletype unit for parallel transfer to or from the accumulator of the processor, see figure 3-9. The control also provides the flags which cause a program interrupt or an instruction skip based upon the availability of the Teletype unit, thus controlling the rate of information transfer flow between the Teletype and the processor as a function of the program. Engineering drawing 11 shows the control and interface connections between the control and the Teletype unit.

In all programmed operations, the Teletype unit is considered two separate devices: a Teletype input device (TTI) from the keyboard or the perforated-tape reader; and a Teletype output device (TTO) for computer output information to be printed and/or punched on tape. Therefore, two device selectors are used, location D26 (5, A7 + B2). One of these is assigned the select code of 03 to initiate operations associated with the keyboard/reader, and the other is assigned the select code of 04 to perform operations

associated with the teleprinter/punch. Corresponding IOT pulses from the two device selectors perform parallel input and output functions. Pulses from the IOP1 pulse trigger the skip control element; pulses from the IOP2 pulse clear the control flags and/or the accumulator; and pulses produced by the IOP4 pulse initiate data transfers to or from the control.

Signals used by the Teletype unit are standard 11-unit-code serial current pulses consisting of marks (bias current) and spaces (no current). Each 11-unit Teletype character consists of a 1-unit start space, eight 1-unit character bits, and a 2-unit stop mark. The 8-bit flip-flop TTI shift register at locations C16, C17, B20, B21, and B18 receive the Teletype characters from the keyboard/reader. The character code of a Teletype character loads into the TTI so that spaces correspond with binary 1s and marks correspond to binary 0s. Upon program command the complement of the contents of the TTI transfers in parallel to the accumulator. Eight-bit computer characters from the accumulator load in parallel into the 8-bit flip-flop shift register TTO at locations A16 through A21 for transmission to the Teletype unit. The TTO clock generates the start space, then shifts the eight character bits into a flip-flop which controls the printer selector magnets of the Teletype unit, and produces the stop mark. This transfer of information from the TTO into the Teletype unit occurs in serial manner at the normal Teletype rate.

A ground IN ACTIVE signal flows from the control circuit of the Teletype incoming line unit module when a Teletype character starts to enter the TTI. This signal clears the TT READER RUN flip-flop, which in turn energizes a relay in the Teletype unit to release the tape feed latch. When released, the latch mechanism stops tape motion only when a complete character has been sensed and before sensing of the next character begins. The KEYBOARD FLAG flip-flop sets and causes a program interrupt when an 8-bit computer character has been assembled in the TTI from a Teletype character. The program senses the condition of this flag with a KSF microinstruction (skip if keyboard flag is a 1, IOT 0301) and issues a KRB microinstruction which clears the AC and the keyboard flag; transfers the contents of the TTI into the AC; and sets the READER RUN flip-flop to enable advance of the tape feed mechanism.

A TELEPRINTER FLG flip-flop sets when the last bit of the Teletype code has been set to the teleprinter/punch, indicating that the TTO is ready to receive a new character from the AC. This flag connects to both the program interrupt synchronization element and the skip control element. Upon detecting the set condition of the flag by the TSF microinstruction (skip if teleprinter flag is a 1, IOT 0401), the program issues a TLS microinstruction which clears the flag and loads a new computer character into the TTO.

Operation of the Teletype incoming line unit TTI requires an input clock signal which is eight times the baud frequency of the Teletype unit. This signal controls the strobing of Teletype information into the TTI during the center of each baud (the most reliable time for sensing) and controls the shifting of information through the flip-flops of the TTI. The Teletype transmitter requires an input clock frequency to be the same as the baud frequency of the Teletype unit. This signal controls the shifting of the TTO and thus determines the timing of the 11-unit-code Teletype character it generates. The three Type R202

Dual Flip-Flops at locations C18 through C20 produce the TTI CLOCK and TTO CLOCK signals. These six flip-flops form a binary counter which provides frequency division of the output from the Type R405 Crystal Clock module at location C21. This frequency division method is used because electronic clocks are not reliable at the low frequency required for Teletype operation. The 7.04-kc frequency of the clock is 64 times the baud frequency of the Teletype unit. Division of the clock frequency by 8 (three binary) flip-flops) yields the TTI CLOCK signal, which is eight times the baud frequency, and division by 64 (six binary flip-flops) yeilds the TTO CLOCK signal, which corresponds with the baud frequency.

3.6.2 Perforated Tape Reader and Control Type 444B

A Digitronics Model 2500 Perforated Tape Reader and a DEC Type 444B Reader Control are standard equipment supplied with every PDP-7 system. The tape reader is a timed-transfer device which senses the holes punched in 5, 7, or 8-channel paper or Mylar-base tape at a maximum rate of 300 lines/sec. When used in the PDP-7 system, the standard input medium is 8-channel tape. The reader control contains an 18-bit output register loaded by the reader, together with all the logic elements necessary for starting and stopping the reader under program control, and sensing the state of the output register. The reader is normally mounted in the center of bay 2, immediately above the operator console. The reader control is located in row C of the KA71A interface package.

The mechanical and electrical operation of the reader is fully described in the manufacturer's manual which is supplied with the PDP-7 system and is identified in the list of Pertinent Documents in chapter 1 of this manual. Therefore, the following paragraphs describe only the logical functions of the reader and control, and the operation of the Type 444B Reader Control.

3.6.2.1 Logical Functions - The program controls entire operation of the reader. When the reader is selected by the appropriate IOT instruction, the brake is released and the clutch engages the capstan to move the tape past the photocells. The feedhold is sensed first, and generates a level transition which causes sensing of the information channels. The sensing of information channels is delayed until the holes have advanced far enough to ensure that punched holes transmit the maximum possible amount of light to the photocells and that tape skew due to worn guides does not cause loss of information. For each hold punched in a given line of tape, a corresponding bit of the RB (reader buffer) is set to 1. Information can be read from the tape and assembled in the reader buffer in either of two modes: alphanumeric or binary.

a. Alphanumeric Mode

The alphanumeric mode, used for reading eight channels of information, is selected by an RSA instruction of the IOT class. Each select instruction causes one line of tape to be read and the information to be placed in bits 10-17 of the RB.

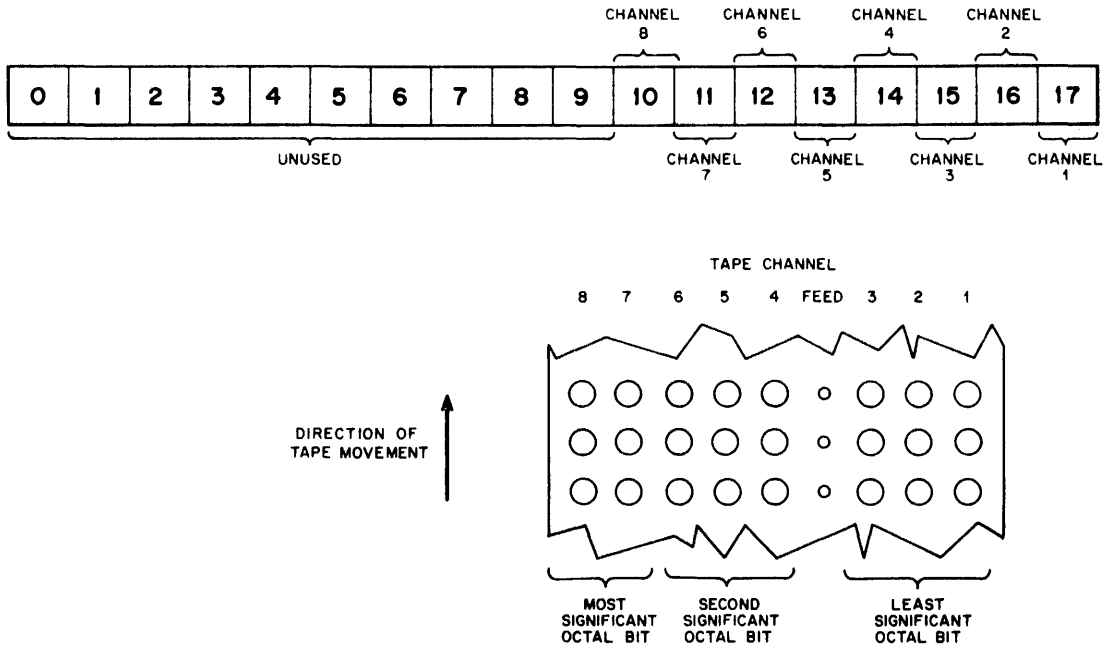
b. Binary Mode

The binary mode, used for reading 18-bit words, is selected by an RSB instruction of the IOT class. One binary word occupies three lines of tape. Each select instruction causes three successive lines of tape to be read, each line containing six bits of binary information. The first line, containing the most significant bits, is read into bits 12-17 of the RB. The RB performs as a 3-stage, 6-bit shift register. When the first line of tape has been read, a shift pulse causes the contents of RB12-17 to be shifted into RB6-11, and simultaneously reads the second line of tape into RB12-17. A second shift pulse shifts the contents of the first line of tape into bits RB0-5, the contents of the second line of tape into RB6-11, and reads the third line of tape into RB12-17. The complete binary character is now assembled in bits RB0-17 and the reader flag is set, indicating that the reader buffer is full. When reading in binary mode, hole 7 is never punched; hole 8 is ignored, but a character is not read unless this hole is punched. The tape format for binary mode is shown in figure 3-10.

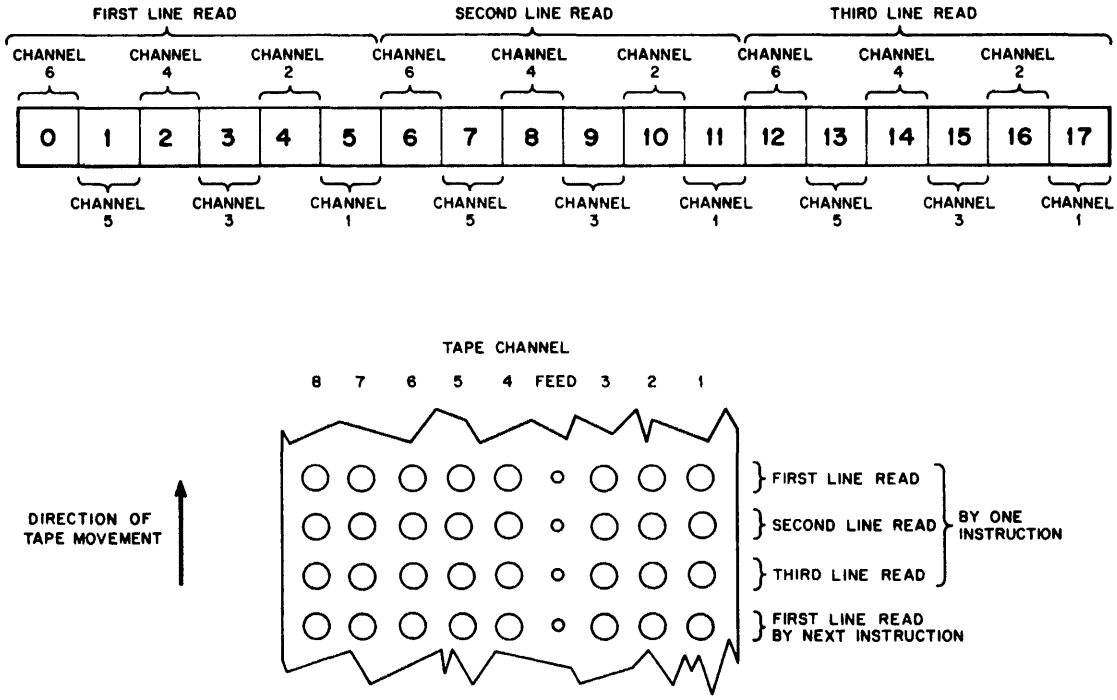
When a program is being stored by use of the READ-IN key, the processor forces the reader into the binary mode and executes a pseudo DAC instruction each time the reader flag is set. If a hole 7 is punched, the processor interprets this as an instruction to stop the reader and to execute the last 18-bit word read.

TABLE 3-3 PERFORATED TAPE READER INSTRUCTIONS

Mnemonic	Octal Code	Effect
RSA	700104	Select reader in alphanumeric mode. One 8-bit character is read and placed in the reader buffer. The reader flag is cleared before the character is read. When transmission is complete, the flag is set.
RSB	700144	Select reader in binary mode. Three 6-bit characters are read and assembled in the reader buffer. The flag is immediately cleared and later set when character assembly is complete.
RSF	700101	Skip if reader flag is set.
RCF	700102	Clear reader flag; then inclusively OR reader buffer into AC.
RRB	700112	Clear reader flag. Clear AC and transfer contents of reader buffer to AC.



Alphanumeric Mode



Binary Mode

Figure 3-10 Tape Format and Reader Buffer Register Bit Assignments

3.6.2.2 Circuit Operations - The logic of the Type 444B Reader Control is shown on engineering drawing BS-D-KA71-0-7. The reader control contains two major groups of logic elements: the reader buffer (RB) and the control logic.

The reader buffer provides temporary storage for alphanumeric or binary characters read by the tape reader. The RB contains two Type R203 FLIP CHIP Triple Flip-Flops, each flip-flop having a direct clear and a DCD set input. These modules are used in bits RB0-RB5. For bits RB6-RB17, Type R202 FLIP CHIP Double Flip-Flops are used, each flip-flop having a direct clear input and DCD set and clear inputs. When reading in alphanumeric mode, bits RB10-RB17 are used. Tape characters are read directly into these flip-flops, and the remaining bits are not used. When reading in binary mode, the input gating causes the register to function as a 3-stage, 6-bit shift register. Figure 3-11 shows a simplified diagram of this configuration. After the first line of tape has been read into bits RB12-RB17, an RD SHIFT 1 is applied to all the DCD input gates of bits RB6-RB17. Bit RB12 determines the condition of bit RB6, and RB17 that of RB11, with a corresponding transfer in intermediate bits. Simultaneously, the second line of tape is read into RB12-RB17. When the third line of tape is ready for reading, RD SHIFT 1 and RD SHIFT 2 pulses are generated simultaneously and applied to the DCD input gates. The RD SHIFT 2 pulse shifts the contents of bits RB6-RB11 into bits RB0-RB5. The RD SHIFT 1 pulse operates in the same manner as before.

The (1) output of each RB flip (ground level) is inverted and appears on terminals of the W020 connector in location C01 and of the W021 connector. Three Type R107 Inverters, each containing seven inverters, are used for this purpose. The connector at location C1 routes the levels to indicators and also provides connections to the IC.

At power turnon, PWR CLR negative pulses from the CP clear the RD BIN, RD RUN, and RD FLAG flip-flops. A BGN pulse at time SP1 of a manual operation, or an IOT 0102 pulse from the device selector also initiates this same clearing action, which establishes initial conditions.

An IOT 0104 command pulse starts the reader. This pulse appears whenever the reader is selected, and triggers a pulse amplifier producing a START pulse which performs three functions:

a. It clears all the reader buffer flip-flops, together with the RD FLAG, RD1 and RD2 flip-flops.

b. It sets the RD RUN flip-flop to 1, thereby starting the tape reader.

c. If bit 12 of the MB contains a 1, the START pulse triggers a DCD gate that sets the RD MODE flip-flop to 1. When this flip-flop is in the 0 state, a ground $\overline{\text{BINARY}}$ level is produced to select the alphanumeric mode. When the RD MODE flip-flop is set to 1, a negative BINARY

level appears to select the binary mode. Note that the RD MODE flip-flop may also be set to 1 when a manual readin operation establishes an RPT (1)B level.

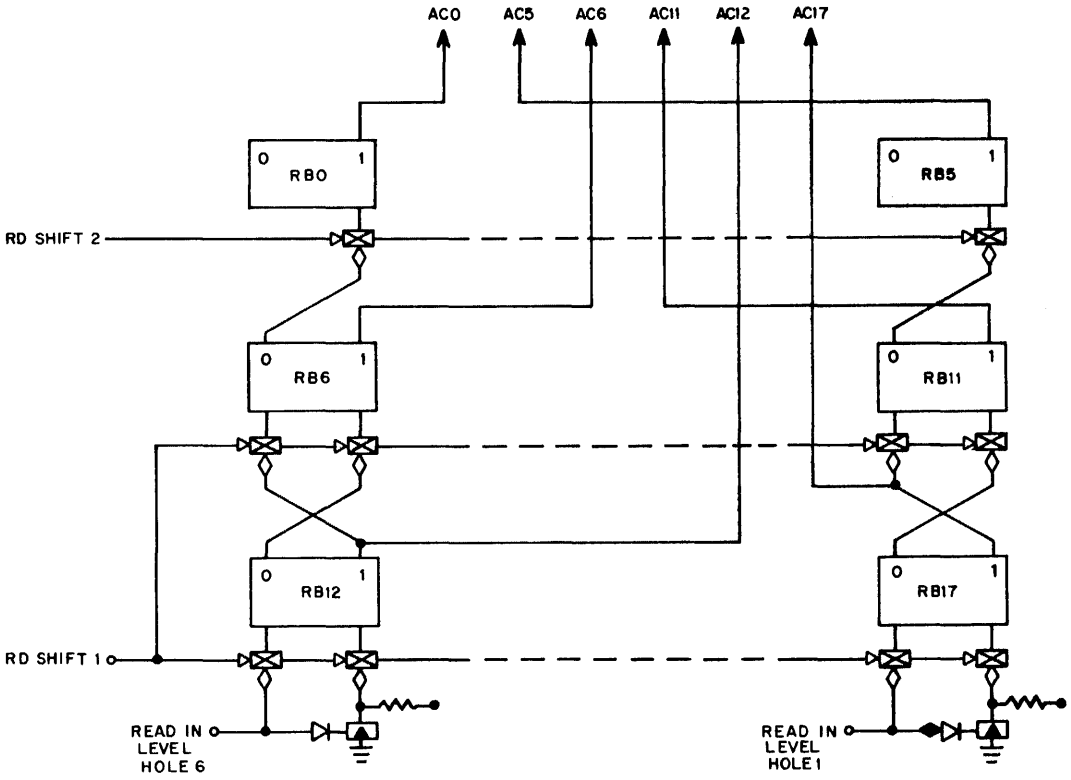


Figure 3-11 Reader Buffer in Binary Mode

Negative levels produced by 1s in the first six bits of the tape are inverted and condition the set DCD gates of flip-flops RB12-RB17. Ground levels produced by 0s are directly applied to the reset DCD gates. The levels produced by holes 7 and 8 condition an additional set of NAND gates which do not open unless strobed. The level transition produced by the feed holde causes Schmitt trigger W501 in module D06 to change state. If the RD RUN flip-flop is set to 1, the output of the Schmitt trigger sets the delay one-shot in module D05. The purpose of this one-shot is to delay the instant at which the reader buffer samples the output of the photocells until the center line of the tape holes coincides with the center of the feed hole. There are two reasons for this. Using a correctly aligned tape, sampling at the leading edge of the feed hole would take place before the other holes were centralized over the photocells, so that the output of the photocells would not yet have reached its maximum value. More important, if worn tape guides have caused skew in the tape, sampling at the leading edge of the feed hole might cause loss of information from holes 7 and 8, as shown in figure 3-12. Delaying the sampling instant ensures that under tolerable conditions of skew all photocells produce some output, so that no information is lost.

When reading alphanumeric mode, the RD STRB output pulse from the one-shot triggers a DCD gate conditioned by a ground $\overline{\text{BINARY}}$ level, and the output of the gate causes an RD SHIFT 3 signal to appear. This pulse, inverted, strobes the hole 7 and hole 8 NAND gates. At the same time, the RD STRB

pulse triggers two other DCD gates conditioned by a BINARY level. One of these gates causes generation of an RD SHIFT 1 pulse; the other causes generation of a RD SHIFT 2 pulse. These RD SHIFT pulses strobe all the DCD input gates of the RB flip-flops and read a line of tape into bits RB10-RB17. This strobe pulse, inverted, sets the RD FLAG flip-flop. Since the NAND gates for holes 7 and 8 are not strobed, these holes are not read. However, hole 8 is always punched, and the negative level, inverted, permits generation of the RD SHIFT signals by conditioning DCD gates.

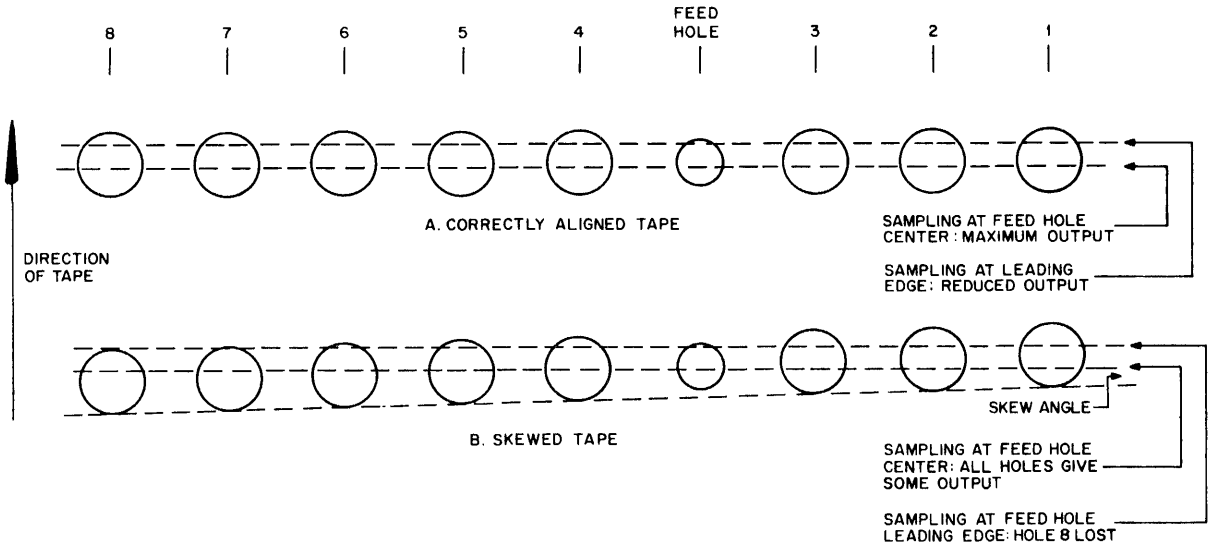


Figure 3-12 Effect of Delayed Sampling

The RD SHIFT 2 pulse which accompanies the reading of the first line of tape sets the RD 1 flip-flop. The output of this flip-flop conditions the DCD set gate of the RD 2 dlip-flop, and the flip-flop is set when the RD SHIFT 2 pulse of the second line of tape appears. The RD 2(1) output conditions the DCD set gate of the RD FLAG flip-flop, and when the third line of tape is read, the accompanying RD SHIFT 2 pulse sets the RD FLAG flip-flop. The setting of the RD FLAG flip-flop indicates to the CP that the reader buffer is full. The positive-going level transition produced by the RD FLAG flip-flop clears both the RD MODE and the RD RUN flip-flops. Clearing the RD MODE flip-flop reestablishes the alphanumeric mode; clearing the RD RUN flip-flop stops the reader.

3.6.3 Tape Punch and Punch Control Type 75D

The Teletype Tape Punch Set (BRPE) and the DEC Type 75D Punch Control are supplied with each PDP-7 as standard equipment. The tape punch is a timed-transfer device capable of punching 5-, 7-, or 8-channel tape at a maximum rate of 63.3 char/sec. In the PDP-7 system the standard output medium is 8-channel tape. The punch control contains an 8-bit data register, which is loaded from the AC through the information distributor. It also contains all the logic elements necessary for starting and

stopping the tape punch and supplying it with the applicable data. The tape punch is mounted in the center bay, above the tape reader. The punch control is located in rows A and B of the KA71A interface package.

The manufacturer's manual supplied with the PDP-7, (see list of Pertinent Documents, chapter 1 of this manual), fully describes the mechanical and electrical operation of the tape punch. Consequently, the following paragraphs describe only the logical functions of the tape punch, and the operation of the punch control.

3.6.3.1 Logical Functions - The program normally controls entire operation of the tape punch. However, the operator may punch leader tape (feed hole only punched) by pressing the PUNCH FEED button on the console or he may force on the punch power by setting the console PUNCH switch. When the first punch IOT instruction selects the tape punch, the punch is turned on and after a 1-sec delay (during which the punch motor comes up to speed), punching begins. Subsequent punch instructions are executed immediately. The punch control functions as a buffer, a control unit, and a solenoid and motor driver for the tape punch. When a tape punch operation is selected by an IOT instruction, a pulse establishes the operating mode of the control (alphanumeric or binary) and causes the transfer of certain of the 1s stored in AC to the buffer register of the punch control via the information distributor. If the mode is alphanumeric, the 1s are transferred from AC bits 10-17. If the mode is binary, the 1s are transferred from AC bits 12-17. The flip-flops containing 1s then enable a series of gates which trigger solenoid drivers and upon receipt of the punch command, a hole is punched in the tape in each channel where a corresponding 1 was present in the AC. When a line of tape has been punched, the buffer register and PUN ACTIVE flip-flops are cleared, and the PUN FLAG is set to indicate to the CP that the punch is ready for a further punching instruction. After the last punch command, the motor remains energized for an additional 5 sec.

a. Alphanumeric Mode

The alphanumeric mode, which a PSA instruction of the IOT class selects, is used for punching 8-channel tape. Each select instruction causes one line of tape, consisting of eight bits, to be punched. A hole is punched in each tape channel whose corresponding bit in the AC is a 1, and a feed hole is always punched.

b. Binary Mode

The binary mode, selected by a PSB instruction of the IOT class, is used for punching 18-bit words. Holes are punched corresponding to bits 12-17 of the PB. Bit 11 (hole 7) is never punched and bit 10 (hole 8) is always punched. This establishes the standard format for binary information on tape. Since only six data bits are punched at a time, a complete 18-bit word requires three lines on the tape and consequently involves three separate PSB instructions.

TABLE 3-4 TAPE PUNCH INSTRUCTIONS

Mnemonic	Octal Code	Effect
PSA	700204	Punch a line of tape in alphanumeric mode. The punch flag is immediately cleared and then set when punching is complete.
PSB	700244	Punch a line of tape in binary mode. The punch flag is immediately cleared and then set when punching is complete.
PSF	700201	Skip the following instruction if the punch flag is set.
PCF	700202	Clear the punch flag.

The following instruction clears the accumulator and causes a line of tape to have only the feed hole punched:

PSA+10	700214	Clear AC and punch.

The following instruction as used on the PDP-4 is also available, but is generally replaced with the more direct PSA.

PLS	700206	Same as PSA.

3.6.3.2 Circuit Operations - Punch Control Type 75D may be divided into the following major functional circuit groups: control logic, punch buffer and solenoid drivers, and motor logic. Engineering drawing KA-71A-0-3 shows all these elements.

a. Control Logic

The operation of the punch is entirely under program control, and the control logic contains all the circuits which interpret a punch instruction and indicate to the CP when a punching operation is complete. PWR CLR pulses generated in the CP at turnon are applied to terminal L of the connector in module A09. These pulses, inverted, trigger a pulse amplifier in module A09 clearing the punch buffer, which is also cleared if an IOT 0202 command pulse and an MB15 (0) level cause a pulse to appear. In both cases the PUN MODE flip-flop is also cleared.

The elements responding to program control are the PUN MODE flip-flop, which determines whether alphanumeric or binary characters will be punched on the tape; the PUN ACTIVE flip-flop, which starts and stops the motor; and the PUN FLAG, which is set to 0 at the beginning of a punching operation and is set to 1 when the punching of a character is complete.

An IOT 0202 command pulse clears the PUN MODE flip-flop. The flip-flop is set by an IOT 0204 pulse, produced by an instruction to punch, if bit 12 of the instruction contains a 1, specifying binary mode. When set, the PUN MODE flip-flop forces a 0 into bit 11 of the punch buffer (hole 7) and a 1 into bit 10 (hole 8). When the PUN MODE flip-flop is in the 0 state (for alphanumeric mode), the corresponding bits of the AC sets bits 10 and 11 of the punch buffer.

An IOT 0204 pulse, produced by an instruction to punch, clears the PUN FLAG and PUN ACTIVE flip-flops. When a character has been punched, a PUN DONE level is produced clearing both these flip-flops and the buffer register. The PUN FLAG (1) level appears at terminal T of the W021 connector in location B30, and is routed to the break control in the CP. The PUN ACTIVE (1) level is utilized in the motor logic.

b. Punch Buffer, Solenoid Drivers, and Synchronization

The punch buffer (PB) is an 8-bit register providing temporary storage for information supplied by the AC. The PB (1) levels condition the solenoid driver input gates. Flip-flops PB10-PB17 are cleared by PWR CLR pulse at power turnon, by an IOT 0202 command pulse, and by the PUN DONE signal produced after the punching of each character. The DCD set gate of each flip-flop is conditioned by the state of the corresponding bit of the AC and is triggered by an IOT 0204 pulse. Thus, binary 1s are transferred from the AC into the PB. 2-input NAND gates control the solenoid drivers. The corresponding PB (1) level conditions one input of each gate; the other input is enabled by a 5-msec signal generated in the synchronization circuits. During this 5-msec period each fully enabled gate causes the associated solenoid driver to energize the solenoid, and a hole is punched in the corresponding tape position. The solenoid driver for the feed hole punch receives only the synchronizing signal and produces a feed hole for every operation.

c. Motor Logic

The punch is turned on and off under program control, but the motor requires 1 sec to attain full speed. To eliminate delay in the execution of successive punch instructions, it is desirable to keep the motor running for 5 sec after a line of tape has been punched, so that a further punch instruction can be executed immediately. The motor logic provides the required control signals for this purpose. The Type R302 Delay One-Shot at location B11 delays the execution of the first punch instruction for 1 sec to allow the motor to come up to speed, and the Type R303 Integrating One-Shot at location R2B4 keeps the motor running for 5 sec after execution of the last punch instruction. These functions are accomplished as follows:

(1) If a punch IOT instruction sets the PUN ACTIVE flip-flop, or if the the console TAPE FEED pushbutton is pressed, a PUN RQ level is produced which sets the integrating one-shot to its unstable state. The negative level produced at the (1) terminal of the integrating one-shot is inverted and causes a relay driver to energize relay K1, thereby starting the motor.

(2) Punching cannot begin until a ground PUN READY level appears at NAND gate output terminal B27N and conditions the DCD input gate of the 1-sec one-shot of the synchronizing one-shot, the PUN READY level appearing only when two inputs of NAND gate module A12 are conditioned by the negative levels. One input is conditioned by the PUN RQ level. The other input is conditioned by the inverted (0) level of the 3-sec delay one-shot at location AB10. When the integrating one-shot is set and starts the motor, the positive-going level transition appearing at the (0) terminal triggers the 1-sec delay one-shot into its unstable state. The output of the delay one-shot, inverted, disables the NAND gate in module A12 thus preventing the generation of a PUN READY level while the motor is gathering speed.

(3) After 1 sec, the motor having attained full speed, the delay one-shot reverts to its stable state. A ground level is inverted which causes a PUN READY level to appear at the output of the gate.

(4) After a character has been punched, the PUN DONE level transition clears the PUN ACTIVE flip-flop, producing a ground $\overline{\text{PUN RQ}}$ which removes the level holding the integrating one-shot in its unstable state. The PUN READY level disappears immediately, preventing further punching. However, the integrating one-shot does not yet change state, and the motor continues to run. At the end of its 5-sec timing period, the integrating one-shot reverts to its stable state, causing relay K1 to be de-energized and the motor to stop. Note that the 5-sec timing period of the integrating one-shot does not begin until clearance of the PUN ACTIVE flip-flop removes the PUN RQ signal holding the integrating one-shot in the unstable state. If a further PUN RQ signal is generated before the end of the timing period, timing action is immediately halted. Thus, the integrating one-shot does not revert to its stable state and stop the motor until a full 5-sec period has elapsed since completion of the last punch instruction.

CHAPTER 4
OPTIONS

4.1 INTRODUCTION

This chapter presents descriptions of standard options not described in other publications. The standard options available with the PDP-7 are divisable into three groups: input/output, processor, and memory.

4.2 INPUT/OUTPUT OPTIONS

Table 4-1 lists the I/O options and the source for detailed descriptions. Chapter 3 describes the channel arrangements for accommodating both medium- and high-speed options (program controlled transfer channels, data channels, direct memory access channels, and automatic priority interrupt channels).

TABLE 4-1 I/O OPTIONS AND APPLICABLE DOCUMENTS

Option	Vendor	Document
Card Reader and Control Type CR01B	DEC	F-75A
Card Reader and Control Type 421	DEC	H-421A/451A
Card Punch and Control Type 40	DEC	F-15(40)
Automatic Line Printer and Control Type 647	DEC	F-75A
DECtape and Control TU55 and 550	DEC	H-TU55 H-550
Magnetic Tape Control Type 57A	DEC	H-57A
Magnetic Tape Transport Type 570	DEC	H-570
Magnetic Tape Transport Type 545	DEC	F-75A
Magnetic Tape Transport Type 50	DEC	Magnetic Tape Equipment Types 50/51/52
Serial Drum System Type 24	DEC	H-24
Incremental Plotter Control Type 350	DEC	PDP-8 Options Manual
Oscilloscope Display Type 34A	DEC	F-15 (34)
Precision CRT Display Type 30D	DEC	F-15 (30E)

TABLE 4-1 I/O OPTIONS AND APPLICABLE DOCUMENTS (continued)

Options	Vendor	Document
Precision Incremental CRT Display Type 340	DEC	H-340
Photomultiplier Light Pen Type 370	DEC	H-370
Analog-to-Digital Converter Type 138E	DEC	H-138E
Multiplexer and Control Type 139E	DEC	H-139E
Analog-to-Digital Converter Type 142	DEC	H-142B
Data Control Type 174	DEC	F-75A
Data Communication System Type 630	DEC	Engineering Bulletin 630
Relay Output Buffer Type 140	DEC	see H-340
Interprocessor Buffer Type 195	DEC	F-75A
Symbol Generators Types 33 and 342	DEC	H-33 and H-342

4.3 PROCESSOR OPTIONS

4.3.1 Automatic Priority Interrupt Type 172B

The optional Automatic Priority Interrupt (API) Type 172B connects up to 16 I/O devices to the program interrupt facility of the PDP-7 processor and allows each device to initiate a program interrupt based on a prewired priority. The API provides direct identification of an interrupting device so that the interrupt subroutine is not required to determine this by scanning device flags. The API also executes multilevel interrupts in which a high-priority device may be granted an interrupt which supersedes an interrupt already in progress. These functions permit servicing more devices with greater speed and efficiency. The API occupies two mounting panels, whose location depends to some extent upon what other options are included in the PDP-7 system.

4.3.1.1 Block Diagram Discussion - The API consists of a control element, a priority chain, and an address selector. The real-time clock of the processor is assigned to channel 17_8 of the API. Figure 4-1 shows the relationship of these elements to each other and to the processor. When a PDP-7 includes the API option, it is connected in place of the real-time clock of the basic system and has a corresponding priority (lower than data break interrupt requests, but higher than program interrupt requests). An interrupt request from a device connected to the API is granted if the following conditions are met:

a. The API is in the enabled condition (by program control).

b. The requesting channel is in the enabled condition (by program control).

c. There is no data interrupt request present or data interrupt in progress.

d. There is no interrupt in progress on a higher priority channel.

e. There is no interrupt in progress on the requesting channel.

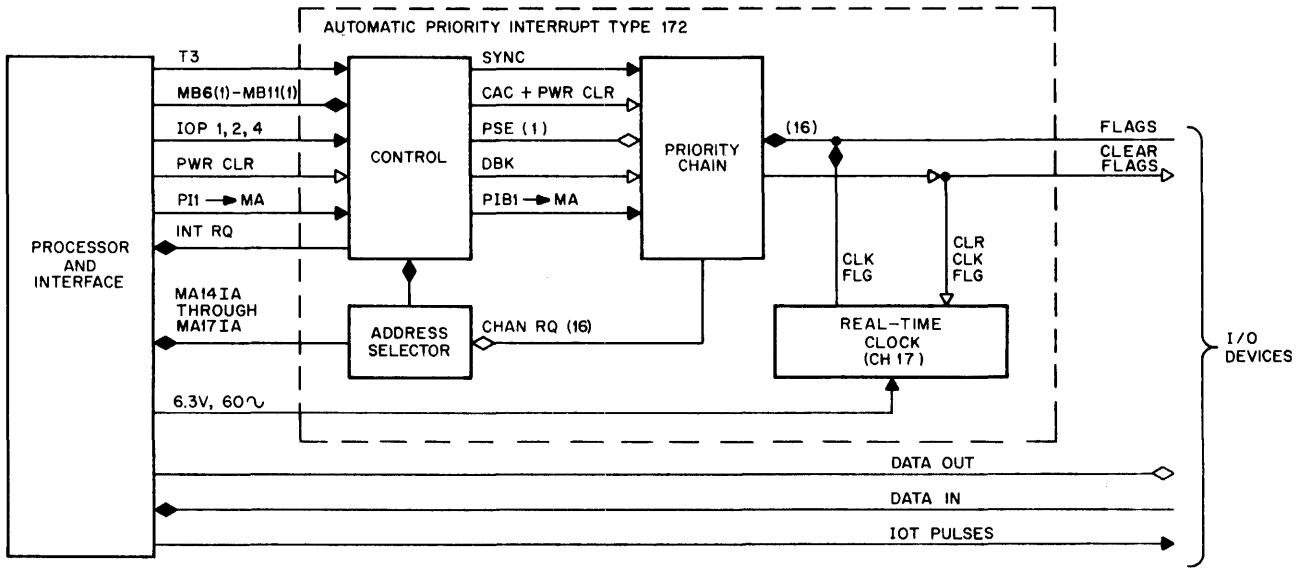


Figure 4-1 Automatic Priority Interrupt Type 172B Block Diagram

Each channel in the API system is assigned a unique, fixed, core memory location (40_8-57_8). When an interrupt is granted, the next instruction is taken from the memory location assigned to the requesting channel.

a. Control

The control element contains all the logic required for enabling or disabling the entire priority system or selected channels, in response to IOT instructions. The control element also generates the interrupt request (INT RQ) level signal, which causes the processor to grant an API interrupt (equivalent to a clock break in the basic system) at the first available opportunity.

b. Priority Chain

The priority chain contains a set of three flip-flops for each channel, designated bXX1, bXX2, and bXX3, where XX represents the channel number. Each bXX1 flip-flop, when set, enables the associated API channel. IOT instructions, in conjunction with the contents of bits 2-17 of the accumulator, sets and clears these flip-flops. At time T3, a

SYNC pulse opens gates which a bXX1(1) level and a CH FLG (channel flag) level condition. The output pulses from gates associated with enabled requesting channels set the associated bXX2 flip-flops. The bXX2(1) output from the highest priority flip-flop generates a CHAN RQ (channel request) level for the associated channel, and disables gates which prevent a CHAN RQ level from being generated by channels of lower priority. Only one channel at a time can generate a CHAN RQ level. The channel request level generated by the requesting channel which carries the highest priority is applied to the address selector element, which generates the memory address assigned to that channel and an INT RQ (interrupt request) level. When the processor grants an API break, it generates a PI1→ MA pulse. The PI1→ MA pulse sets the address which the address selector generates into the MA of the processor, and transmits it to the API where it sets the bXX3 (hold break) flip-flop of the requesting channel. The level transition that occurs when the bXX3 flip-flop is set to 1 clears the device flag. This flip-flop remains set until the control element generates a DBK (debreak) pulse. It is cleared by a CAC (clear all channels) instruction.

c. Address Selector

The address selector consists of four NOR gates which set 1s or 0s into bits 14-17 of the MA to produce the memory address of the channel in which a CHAN RQ level is generated. The channel address is transferred into the MA at time T1 of the API break cycle. The API address selector also contains circuits that assure that MA121A is always a 1 and MA131A is always a 0 when the API is granted an interrupt; hence the memory address range of 40_8-57_8.

d. Real Time Clock

The real-time clock consists of a Schmitt trigger, a pulse amplifier, and a clock flag flip-flop. The Schmitt trigger input receives a 6.3 vac, 60 cps signal from a processor power supply, and the trigger output is coupled to the pulse amplifier, which produces 100-nsec pulses at the rate of 60 per sec. Each clock pulse sets the clock flag flip-flop and, if its channel is enabled, requests an API break. One channel ($CH17_8$) if assigned to the real-time clock and one is assigned for overflow from the core memory location containing the clock count.

4.3.1.2 Logical Functions

a. Channel Allocation

The API provides 16 automatic interrupt channels arranged in a priority chain so that channel 00_8 has the highest priority and channel 17_8 has the lowest priority. Each channel is assigned a unique, fixed memory location in the range 40_8 ($CH00_8$) through 57_8 ($CH17_8$). Each

I/O device is assigned a unique channel in order of device operating speed. The higher-speed devices are assigned to the higher-priority channels. The priority chain guarantees that if two or more devices request an interrupt concurrently, the first interrupt is granted to the device with the highest priority. When this device has been serviced, further interrupts are granted to the other devices, in order of priority.

b. Multi-Instruction Subroutine Mode

This mode is generally used to service an I/O device that requires control information from the PDP-7. Such devices are alarms, slow electromechanical devices, teleprinters, punches, etc. Each device requires a servicing subroutine that includes instructions to manipulate data and give further instructions, such as continue, halt, etc., to the interrupting device. When an interrupt is granted, the contents of the channel memory location are transferred to the MB and executed. If the instruction executed is JMS Y, the system operates in the multi-instruction subroutine mode. The contents of the program counter and the condition of the link are stored in location Y, and the device-servicing subroutine starts in Y + 1. (Note that it is often useful to store the contents of the AC before servicing the device and to restore the AC prior to exiting from the servicing routine.)

The interrupt flag is normally lowered by the 172, but can be lowered by an IOT instruction if desired. Program control now rests with the servicing routine.

A return to the main program is accomplished by an instruction sequence that restores the AC and link, issues a debreak IOT, and gives a jump indirect to location Y (where the contents of the PC prior to interrupt are stored). The debreaking IOT requires no channel designator, since the interrupt priority chain automatically releases the correct channel and returns it to the receptive state. This IOT normally inhibits all other interrupts for one memory cycle to ensure that the jump indirect Y is executed immediately.

The following program example illustrates the action that takes place during the multi-instruction subroutine mode. Assume an interrupt on channel 03.

Memory Location	Instruction	Operation
1000	ADD 2650	Instruction being executed when interrupt request occurs.
0043	JMS 3000	Instruction executed as a result of interrupt on channel 03. The JMS determines multi-instruction mode.
3000	---	The link, condition of the extend mode, and the PC are stored in location 3000.
3001	DAC 3050	First instruction of servicing routines stores AC.

Memory Location	Instruction	Operation
3002	---	Instructions servicing the interrupting in/out device.
3003	---	
3004	---	
3005	---	
3006	---	
3007	LAC 3050	Restores AC for main program.
3010	DBR	Debreaking IOT releases channel.
3011	JMP I 3000	Return to main program sequence.
1001	---	Next instruction executed from here unless another priority interrupt is waiting.

c. Single-Instruction Subroutine Mode

In some instances, it is desirable for the PDP-7 to receive information from an external device but not to send control information to the device, such as in the counting of real-time clock pulses to determine elapsed time. The single-instruction subroutine mode simplifies programming a counter.

An interrupt request is subject to the same conditions as in the multi-instruction mode, and the appropriate memory location is addressed as described previously. Then the single-instruction subroutine mode is entered if the channel memory location does not contain a JMS instruction. Normally the instruction is ISZ. In any case, since the signal instruction constitutes the entire subroutine, the interrupt system automatically lowers the interrupt flag, debreaks the interrupting channel, and returns the channel to the receptive condition.

If the ISZ instruction is used, the API acknowledges only the incrementing operation and neglects the skip to avoid changing the contents of the program counter. If an overflow results from the incrementing, a flag is set. This flag can be entered in another channel or the interrupt system to cause a further program interrupt.

The following program coding illustrates operation in the single-instruction subroutine mode. Assume an interrupt on channel 06.

Memory Location	Instruction	Operation
1200	DAC 1600	Operation being executed when interrupt occurs.
0046	ISZ 3200	Instruction executed as a result of break on channel 06. If overflow, flag is set, PC not changed.
1201	LAC 1620	Next instruction in sequence of main program.

d. Automatic Priority Interrupt Instructions

The following instructions are added to the PDP-7 with the installation of the Type 172 API option. Some instructions, for example CAC and ASC, can be microprogrammed.

Octal Code	Mnemonic	Operation
CAC	705501	Clear all channels: turn off all channels.
ASC	705502	Enable selected channel(s). AC bits 2 through 17 are used to select the channel(s).
DSC	705604	Disable selected channel(s). AC bits 2 through 17 are used to select the channel(s).
EPI	700004	Enable automatic priority interrupt system. Same as real-time clock CLON.
DPI	700044	Disable automatic priority interrupt system. Same as real-time clock CLOF.
ISC	705504	Initiate break on selected channel (for maintenance purposes). AC bits 2 through 17 are used to select the channel.
DBR	705601	Debreak. Returns highest priority channel to receptive state. Used to exit from multi-instruction subroutine mode.

AC bits 0 to 1 are available for expansion of the basic automatic priority interrupt system to 4 groups of 16 channels.

4.3.1.3 Circuit Operations

a. Control

The control circuits generate seven conditioning levels and ten command pulses for the operation of the API system. The logic circuits which produce these signals are shown on engineering drawing 172B-2.

The PWR CLR + CAC positive pulse provides a means of collectively clearing all flip-flops contained in the API, either automatically at power turn-on or under program control. The PWR CLR + CAC positive pulse appears at pulse amplifier output terminal E3K. This pulse amplifier is triggered either by PWR CLR POS pulses applied to DCD gate E3E, F, or by IOP 1 pulses generated in the processor and inverted by inverter LMN of module E7 (C1, 172B-0-2). The inverted pulse is applied to DCD input E3H; and, if the level input of this gate is conditioned by an IO 55 level, the pulse amplifier is triggered and generates the PWR CLR + CAC pulse.

The IO 55 and IO 56 levels are the basic enabling and disabling levels for the entire API system. These levels are generated by decoding the content of bits 6 through 11 of the MB in NAND gates at location F3 and F4. The IO 55 assertion levels appear at terminals F3E (negative) and F3D (ground). The IO 56 levels appear at terminals F4E (negative) and F4D (ground).

The PSE(1) (priority system enable) negative level conditions the NAND gates associated with channel 00. The PSE(1) ground level conditions a DCD gate, which resets flip-flop b003 in the priority chain when triggered by a COMMON DEBREAK pulse. The PSE(1) levels are generated by the PS ENABLE flip-flop, which is set by an EPI (enable priority interrupt) instruction and reset by a DPI (disable priority interrupt) instruction. These IOT instructions contain a 1 and a 0, respectively, in bit 12, which conditions NAND gates JKL and DEF in module A12. The IOT 0004 command pulse, generated in the device selector, triggers whichever gate is conditioned and sets or resets the flip-flop. The PS ENABLE flip-flop must be set by an EPI instruction before the API can initiate an interrupt from any channel.

The ASC 5502 command pulse appears at pulse amplifier output terminal E3U. An IOP2 pulse generated in the CP triggers this pulse amplifier which inverter PRS of module E7 inverts. The inverted pulse is applied to DCD input E3P and triggers the pulse amplifier when an IO 55 ground level conditions the gate. The ASC 5502 pulse sets all bXX1 flip-flops of the priority chain whose DCD set gates are conditioned by a 1 in the corresponding bit of the AC.

The DSC 5604 command pulse appears at pulse amplifier output terminal E5K. An inverted IOP 4 pulse applied to DCD input 5E triggers this pulse amplifier when the DCD gate is conditioned by an IO 56 ground level. The DSC 5604 pulse resets all bXX1 flip-flops of the priority chain whose DCD reset gates are conditioned by a 1 in the corresponding bit of the AC.

The ISC 5504 command pulse appears at pulse amplifier output terminal E4K. An inverted IOP 4 pulse applied to DCD input terminal E4E triggers this pulse amplifier when the the gate is conditioned by an IO 55 ground level. The ISC 5504 pulse sets the bXX2 flip-flop of any channel selected by the insertion of a 1 in the corresponding bit of the AC. The setting of the bXX2 flip-flop initiates a break request by the selected channel (or by the highest priority channel if more than one has been selected). This command initiates a break request on the selected channel or on the highest priority channel selected, independent of the channel enable/disable conditions. The channel must be disabled if there is no device connected to it. If a device is connected to the channel, the channel can be enabled, but the program must consider the status of the external device. The ISC instruction allows diagnostic routines to initiate a break on any channel, independent of external operations.

The negative INSURE DEBREAK level is generated by the INSURE DEBREAK flip-flop and appears at terminal A15J when the flip-flop is set to 1. This level is applied to terminal J30P of the break control in the CP and forces a $\overline{\text{BK RQ}}$ condition for one cycle at the end of an API break. This ensures that an indirectly addressed JMP instruction providing exit from a break routine will be executed immediately. Any instruction that generates a DBK (debreak) command sets the INSURE DEBREAK flip-flop which is reset to 0 by timing pulse T3 of the following cycle.

The DEBR (debreak) command pulse appears at pulse amplifier output terminal E5 (C3, 172-0-2). This pulse not only sets the INSURE DEBREAK flip-flop, but also triggers a pulse amplifier to produce a COMMON DEBREAK command pulse in the priority chain. The DEBR command pulse is generated by either of the following conditions:

(1) An IOP 1 pulse, inverted, is combined with an IO 56 ground level in DCD gate PR of module E5 to trigger the pulse amplifier.

(2) The INT RECOGNIZED flip-flop is set during time T1 of the API break cycle by a PI1 → MA pulse generated in the break control of the CP. The INT RECOGNIZED (1) negative level conditions one input of the NAND gate in module E8. If two other inputs are conditioned by an F (fetch) level and a $\overline{\text{JMS}}$ level, at time T5 of the fetch cycle the gate is triggered and causes the pulse amplifier to generate the DBK pulse. If the following cycle is also to be a fetch, the F SET level from the major state generator is combined with timing pulse T7 of the current cycle to reset the INT RECOGNIZED flip-flop.

The OVERFLOW FLAG (1) level is generated during an API break in which the instruction in the assigned memory location of the requesting channel is ISZ. If the indexing operation causes an overflow, an MBO CRY (B) pulse triggers gate NPR of module A12 and sets the OVERFLOW FLAG flip-flop. The (1) output is applied to another channel of the priority chain and initiates a break request. The OVERFLOW FLAG flip-flop is cleared when the interrupt is granted.

A SYNC command pulse appears at pulse amplifier output terminal E9N. This pulse amplifier is triggered by NAND gate RNPV of module E8 which is operated at time T3 of each cycle in which the $\overline{\text{INT REC}}$ level and the $\overline{\text{IO DEVICE 56}}$ are both present. The presence of these levels assures that no SYNC pulse will be issued when the API tries to debreak (DEBR) and return to the main program sequence. The SYNC command pulse sets the bXX2 flip-flop of all API channels which have been enabled and are requesting an interrupt with a CH FLAG level.

The PIB1 → MA pulse appears at pulse amplifier output terminal E9H. This pulse amplifier is triggered when a PI1 → MA pulse appears, indicating that an interrupt has been granted. The PI1 ⇒ MA pulse is generated in the processor break control circuits at time T1 of the break cycle and forces the major state generator to the fetch state. This pulse appears at terminal IL 25H and is identical to the CLOCK 7 → MA pulse of the basic PDP-7 system. The PI B1 → MA pulse is applied to all channels of the priority chain, thereby setting flip-flop bXX3 of the highest priority enabled. Setting of this flip-flop turns on the channel and clears the flag of the device to which an interrupt has been granted.

b. Address Selector

The address selector circuits generate negative levels which condition the input gates of bits 14 through 17 of the MA, thereby setting the memory address assigned to the requesting channel into the MA. The address selector circuits also generate the INT RQ level which sets the API SYNC (CLK SYNC in the basic system) flip-flop of the break control (engineering drawing KA77-A-14). The CHAN RQ (channel request) levels of all channels in the priority chain are applied to the four NOR gates in modules A16, A17, A18, and A19. Only the highest priority requesting channel generates a CHAN RQ level, so that only one address at a time can be set up. In addition to the four MA addressing levels generated by the NOR gates, an MA121A level is generated with each address by disconnecting the ground jumper on terminal P of module F27 in the MA (KA-77-15). This wiring modification, in conjunction with the fact that MA131A is never set to 1 by the PIB → MA pulse (KA77-15) produces the desired range of memory locations (40_8-57_8).

The INT RQ (interrupt request) level appears at terminal A14M. Any address selected by a selected channel causes one or more of the NOR gates to apply a ground output level to the NOR gate in module A20. The INT RQ level is then generated from A20D, unless the PS ENABLE flip-flop is in the 0 state. In that case, the negative PSE (0) level is inverted in module A14 and grounds the INT RQ line.

c. Priority Chain

Each channel of the priority chain consists of three flip-flops, four NAND gates, an inverter, and a pulse amplifier connected in a configuration that is identical in each channel. The logic of the priority chain is shown on engineering drawing 172B-0-3. Only channel 01 is described below, since all other channels operate in an identical manner.

Channel 01 is enabled when flip-flop b011 is set. The setting pulse is provided by a DCD gate conditioned by a 1 in bit 3 of the AC and triggered by an ASC 5502 command pulse from the control element. Similarly, the channel is disabled when flip-flop b011 is reset by

the combination of a 1 in bit 3 of the AC and a DSC 5604 command pulse from the control element. When channel 01 is enabled under program control, the b011(1) level conditions one input of NAND gate KLMN in module E14(C2, 172B-0-3). Another input is conditioned by a CH 1 FLG (channel 1 flag) level generated in the associated I/O device. At time T3 of the computer cycle, a SYNC pulse from the control element triggers the NAND gate; and the output of the gate sets flip-flop b012. This flip-flop may also be set by the combination of a 1 in bit 3 of the AC and an ISC 5504 command pulse from the control element. Use of the ISC instruction causes a break to be initiated on the selected channel without a prior enabling instruction.

Three levels condition NAND gate KLMN in module C10. The input at terminal M is a negative level indicating that channel 01 is enabled and that the associated device has requested a break. The input at terminal L is a negative level indicating that no break is already in progress on this channel. The input at terminal K is a negative level indicating that no break is in progress on a channel or higher priority, and that the API system as a whole is enabled. If all these conditions are met, the gate becomes fully enabled and generates a CHAN 01 RQ (channel 01 request) ground level at terminal C10N. The CHAN 01 RQ level is applied to the control element, where it generates the memory address assigned to channel 01, as well as an interrupt request level, which is applied to the break control of the CP. When the interrupt is granted, the break control generates a command pulse which sets the API address levels into the MA, and causes the control element to generate a PIB1 pulse. This pulse triggers NAND gate DEFH in module C10, the priority level and a b012(1) level have already conditioned the gate. The output of the gate sets the b013 flip-flop to 1. The positive-going level transition which appears at terminal B10S of this flip-flop triggers a pulse amplifier in module B9, and produces a CLR FLG 1 pulse at terminal B9U. This pulse clears the I/O device flag to indicate that an interrupt has been granted.

Note that any bXX2 flip-flop, which is in the 1 state, produces a ground level at terminal H, thereby disabling the associated NAND gate RSTU. The inverted output of a disabled RSTU gate disables inputs D, K, and R of the three NAND gates associated with the next channel of lower priority. This prevents the lower priority channel from generating either a CHAN RQ or a CLR FLG signal. When the flags of several devices are set concurrently, the SYNC pulse sets the bXX2 flip-flop in each of these channels. However, the CHAN RQ levels appear one by one, in order of channel priority.

All flip-flops in all channels are cleared by a CAC + PWR CLR pulse generated in the control element at power turn-on or when a CAC (clear all channels) instruction is executed.

While an interrupt is in progress on channel 01, the b013 flip-flop remains set. At the end of the interrupt, both flip-flops b013 and b012 are reset to 0. A COMMON DEBREAK pulse from the control element resets flip-flop b013 and the level transition of b013 resets flip-flop b012. Note that the COMMON DEBREAK pulse triggers a DCD gate conditioned by a ground level from the channel of next higher priority. Therefore, although the COMMON DEBR pulse is applied to all channels, only the channel to which the interrupt was granted is cleared.

4.3.2 Data Interrupt Multiplexer Type 173

Data Interrupt Multiplexer Type 173 consists of 60 FLIP CHIP modules contained in two mounting panels. When this option is added to a standard PDP-7 system, the location of the mounting panels depends somewhat upon the number and type of other optional equipment in the system. When the 173 option is designed into a specific PDP-7 system, convenience may require that the multiplexer be located in a specific portion of the console. Module map 173-4 shows the locations of modules within the panels. Data Interrupt Multiplexer Type 173 permits the direct transfer of information between the PDP-7 core memory and one of four high-speed I/O devices which can supply 15 address lines, 18 data lines, a request line, and a transfer direction line. The multiplexer services the devices in a preset priority order and routes the address and data supplied by each device into the data interrupt channel of the standard PDP-7 system. The data interrupt channel has priority over all other interrupt requests. When a data break is granted by the central processor on completion of the current instruction, the transfer takes place during one computer cycle, under the control of the I/O device. The maximum combined transfer rate of four devices connected to the CP through the multiplexer is 570,000 18-bit words per second.

4.3.2.1 Logical Functions - Figure 4-2 shows a block diagram of the logical elements of the data interrupt multiplexer and their relationship to the central processor. When one or more of the devices connected to the multiplexer generate a channel DATA RQ level (−3v), the multiplexer control transmits to the CP a DATA RQ level which causes the DATA SYNC flip-flop in the interrupt control to be set at time T5 DLY (delayed) of the current cycle. At time T6 of the same cycle, the multiplexer control selects the device having the highest priority. When the central processor reaches an "instruction done" stiuation and grants a break cycle, the following events take place:

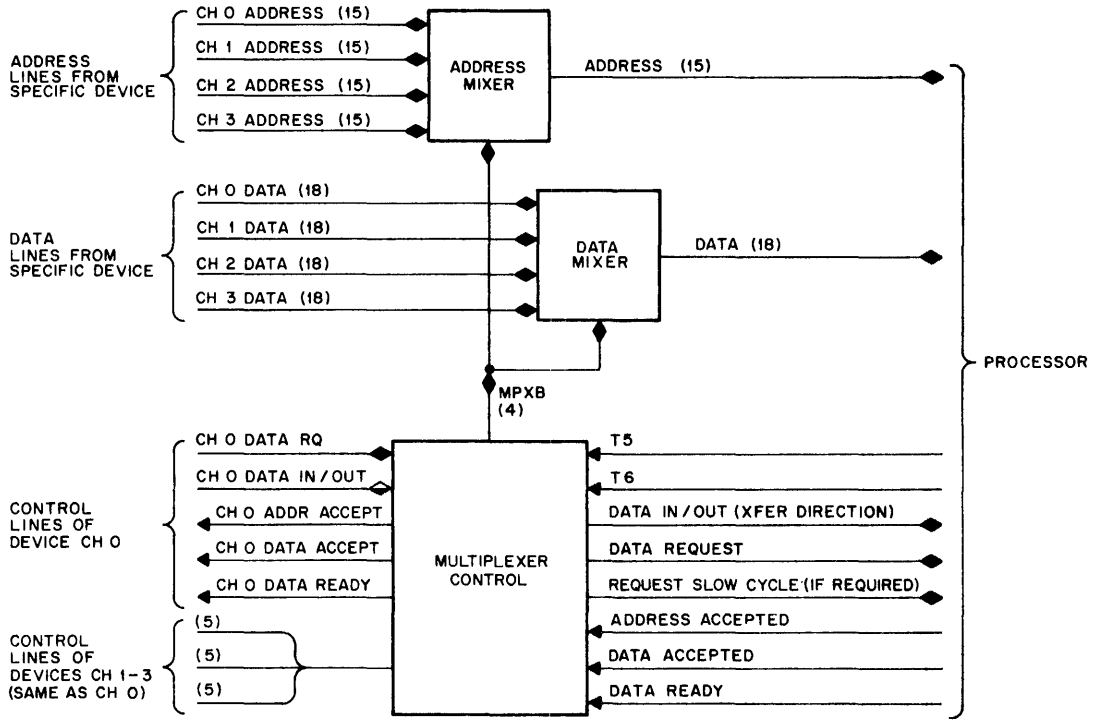


Figure 4-2 Data Interrupt Multiplexer Type 173 Block Diagram

a. At time T1 of the break cycle, the processor transfers the address supplied by the requesting device into the MA, and the multiplexer returns a negative ADDR ACC (address accepted) pulse to the requesting device.

b. At time T3, if an in transfer has been specified, the processor transfers the data supplied by the device into the MB, and the multiplexer returns a DATA ACC (data accepted) pulse to the requesting device.

c. At time T3, if an out transfer has been specified, the information that was stored in the addressed memory cell is held in the MB, and the multiplexer returns a DATA RDY (data ready) pulse to the requesting device, indicating that the requested data is ready for sampling.

d. At time T5 of the multiplexer the priority chain is cleared and the processor interrogates the DATA RQ line.

e. If the DATA RQ line is still a -3v, the processor grants another break cycle, and the events described in a through d are repeated until all requesting devices have been serviced in order of priority. If the DATA RQ line is at ground, indicating that there is no further data request, the processor fetches and executes the next programmed instruction.

4.3.2.2 Circuit Operations - The following discussion of the detailed operation of Data Interrupt Multiplexer Type 173 is based on engineering logic drawings 173-2 and 173-3. Reference is also made to the break control of the central processor, shown on engineering logic diagram KA77-14.

a. Data Interrupt Multiplexer Control

Each of the four I/O devices which may be connected to the multiplexer must supply a −3v CH X DATA RQ level when it is ready to receive or transmit data. The four request lines are OR combined in module A3 of the multiplexer (173-2:C5). A data request from any or all of the four I/O devices results in the transmission of a negative DATA RQ level to the break control of the central processor. This DATA RQ level is AND combined with timing pulse T5 DLY to set the DATA SYNC flip-flop (KA77-14). In the break control, the DATA SYNC (1) level is inverted in NOR gate N21 (A7,14) to produce a negative BK RQ level which is applied to the major state generator. When the processor reaches an "instruction done" situation, the major state generator establishes a break state. The B (break) and DATA SYNC (1) levels are combined to produce a DATA·B level.

In the multiplexer, the CH X DATA RQ level conditions a gate which timing pulse T6 of the current computer cycle triggers to set the associated MPX flip-flop. There are four flip-flops, designated MPX0 through MPX3. The inverted (1) level of each flip-flop holds all flip-flops of lower priority in the 0 state by pull-over action. Thus, only one flip-flop at a time can be set, and if two or more I/O devices have generated a DATA RQ level concurrently, the MPX flip-flop which is set at time T6 will be that associated with the device of highest priority.

The MPX (1) level performs five functions, as follows:

(1) It conditions the address mixer gates which connect the address lines of the requesting device to the MA.

(2) It conditions the data mixer gates which connect the data lines of the requesting device to the MB.

(3) It is NAND combined in module A6 with the CH RQ IN level to produce a DATA IN level for transmission to the break control of the processor.

(4) It is applied to one input of a two-input diode AND gate in a Type R141 module at location A5. The outputs of the seven gates in this module are NOR combined. As supplied, the second input of each gate is disabled by a ground connection; however, if any of the four I/O devices require a slow cycle, the associated gate may be conditioned by the CH DATA RQ and MPXB negative levels to generate a negative RQ SLOW CYC level for transmission to the processor timing circuits.

(5) It is applied to the input of a bus driver, whose output conditions three NAND gates contained in a Type R111 module. The Type R111 modules for channels 0 through 3 are at locations C12 through C15, respectively. In each channel, an ADDR ACC (address accepted) pulse from the processor triggers one NAND gate; the output of the gate causes an associated Type W607 pulse amplifier to transmit a CHX ADDR ACC (channel address accepted) pulse to the requesting device. A DATA ACC (data accepted) pulse triggers these gates during an inward transfer, causing the associated pulse amplifier to transmit a CHX DATA ACC pulse to the requesting device. A DATA RDY (data ready) pulse triggers the third gate during an outward transfer causing the associated pulse amplifier to transmit a CHX DATA RDY pulse to the requesting device. The three control pulses (ADDR ACC, DATA ACC, and DATA RDY) are generated in the processor (as the DATA ADDR → MA, DATA INFO → MB, and MB INFO → OUT pulses, respectively) and are transmitted to the multipliexer control.

At time T5, timing pulse T5 (inverted) applied to the direct clear inputs of all four MPX flip-flops resets them to 0. If no other I/O device has generated at the CH DATA RQ level in the meantime, the DATA RQ line is at ground and permits timing pulse T5 DLY to clear the DATA SYNC flip-flop in the break control. At the conclusion of the break cycle, the processor then fetches and executes the next programmed instruction. If, however, a further CH DATA RQ level has been generated, the DATA SYNC flip-flop remains set and the processor grants further data break cycles until all requesting devices have been serviced in order of priority.

b. Address Mixer and Data Mixer

The address mixer consists of 15 Type R141 Diode Gate modules at locations B10 through B24, and 3 Type B105 Inverter modules each containing 5 inverters. Each Type 141 module contains seven 2-input diode AND gates whose outputs are NOR combined. Three of these diode AND gates are unused. In the remaining four gates, one input is conditioned by one of the MPXB levels; the other input is conditioned by an address line from the associated device. The ground level that appears at terminal D of the Type R141 module when one of its gates is enabled is applied to an inverter of the Type B105 module. The resulting negative level conditions the input gate of the corresponding bit of the MA.

The data mixer is similar in operation to the address mixer, except the device data lines condition the input gates and there are 18 bits instead of 15. The Type 141 modules are located at positions A7 through A24, and the Type B105 modules at positions B3, B4, C1, and C2. Each inverter in each mixer is equipped with a 15-ma clamped load; these loads are contained in Type W005 modules at locations C6 through C8.

4.3.3 Extended Arithmetic Element (EAE) Type 177

A standard option for the PDP-7, the extended arithmetic element (EAE) enables the processor to perform arithmetic operations at faster speeds. With the EAE option installed, the processor can perform parallel arithmetic operations. The programmer's instruction repertoire is also considerably expanded. Certain EAE instructions being augmented are microprogrammed to perform several nonconflicting logical operations with one instruction. Other EAE commands are microcoded to perform specific arithmetic operations such as multiply, divide, normalize, and shift. The arithmetic commands allow the EAE to operate asynchronously to the processor main timing chain permitting computations to be performed in the minimum possible time.

The EAE logic consists of an 18-bit multiplier-quotient register (MQ), a 6-bit step counter (SC), two 1-bit sign registers (EAE sign and EAE AC sign), timing and control logic (EAE states, EAE register control, and EAE main time chain) and data buffering logic (AC inverters). The four rows of EAE logic are installed below the operator console in bay 2. The contents of the MQ register are displayed on the MULTIPLIER QUOTIENT indicators located on the operators console below the ACCUMULATOR indicators.

4.3.3.1 Instructions - There are two classes of EAE instructions, setup and arithmetic. The setup instruction performs as an OPR instruction and is able to perform several nonconflicting logical operations during a normal computer fetch cycle. The EAE setup instruction consists of the op code 64_8 in bits 0 through 4 and the command code 0_8 in bits 9 through 11. Bits 5 through 8 and 12 through 17 are used for microprogrammed logical operations. The arithmetic class of EAE instructions performs as specific arithmetic operations and operates in an argument fetch cycle. The EAE arithmetic instructions consist of op code 64_8 in bits 0 through 4, and the specific arithmetic command listed below in bits 9 through 11.

1_8 Multiply

2_8 Unassigned

3_8 Divide

4_8 Normalize

5_8 Long Shift Right

6_8 Long Shift Left

7_8 Accumulator Shift Left

Bits 5 through 8 are used for logical operations and bits 12 through 17 contain the number of steps in the arithmetic command. For specific bit assignments refer to Table 4-2 EAE Bit Assignments and Operations.

TABLE 4-2 EAE BIT ASSIGNMENTS AND OPERATIONS

Bit Positions	Bits	Function
0,1,2,3	1101	EAE operation code.
4	1	Place the AC sign in the link. Used for signed operations.
5	1	Clear the MQ.
6	1	Read the AC sign into the EAE AC sign register prior to carrying out a stepped operation. Used for the signed operations multiply and divide.
6,7	10	Take the absolute value of the AC. Takes place after the AC sign is read into the EAE AC sign.
7	1	Inclusive OR the AC with the MQ and read into MQ. (If bit 5 is a 1, this reads the AC into the MQ).
8	1	Clear the AC.
9,10,11	000	Setup. Specifies no stepped EAE operation, and enables the use of bits 15,16, and 17. It is used as a preliminary to multiplying, dividing, and shifting signed numbers. Execution time is one cycle.
9,10,11	001	Multiply. Causes the number in the MQ to be multiplied by the number in the memory location following this instruction. If the EAE AC sign register is 1, the MQ will be complemented prior to multiplication. The exclusive OR of the EAE AC sign and the link will be placed in the EAE sign register (the sign of product). The product is left in the AC and MQ, with the lowest order bit in MQ bit 17. The program continues at the location of this instruction plus two. At the completion of this instruction the link is cleared and if the EAE sign was 1, the AC and MQ are complemented. The step count of this instruction should be 22 for a 36-bit multiplication, but can be varied to speed up the operation. The execution time is 4.2 to 8.7 μsec, depending on number of 1 bits in the MQ.
9,10,11	010	This is an unused operation code reserved for possible future expansion.
9,10,11	011	Divide. Causes the 36-bit number in the AC and MQ to be divided by the 18-bit number in MB following the instruction. If the EAE AC sign is 1, the MQ is complemented prior to starting the division. The magnitude of the AC is taken by microprogramming the instruction. The exclusive OR of the AC sign and the link are placed in the EAE sign. The part of the dividend in the AC must be less than the divisor or overflow occurs. In that case the link is set at the end of the divide;

TABLE 4-2 EAE BIT ASSIGNMENTS AND OPERATIONS (Continued)

Bit Positions	Bits	Function
		otherwise, the link is cleared. At the completion of this instruction, if the EAE sign was a 1, the MQ is complemented; and if the EAE AC sign was 1, the AC is complemented. Thus, the remainder has the same sign as the dividend. The step count of this instruction is normally 23 (octal) but can be decreased for certain operations. The execution time is 3.5 μsec in the case of divide overflow or from 9.0-12.6 μsec otherwise.
9,10,11	101	Long right shift. Causes the AC and MQ to be shifted right together as a 36-bit register the number of times specified in the step count of the instruction. On each step the link fills AC bit 0, AC bit 17 fills MQ bit 0, and MQ bit 17 is lost. The link remains unchanged. The time is 0.1 n + 1.6 μsec, where n is the step count.
9,10,11	110	Long left shift. Causes the AC and MQ to be shifted left together the number of times specified in the step count of the instruction. On each step, MQ bit 17 is filled by the link; the link remains unchanged. MQ bit 0 fills AC bit 17 and AC bit 0 is lost. The time is 0.1 n + 1.6 μsec, where n is the shift count.
9,10,11	100	Normalize. Causes the AC and MQ to be shifted left together until either the step count is exceeded or AC bit 0 $\neq$ AC bit 1. MQ bit 17 is filled by the link, but the link is not changed. The step count of this instruction would normally be 44 (octal). When the step counter is read into the AC, it contains the number of shifts minus the initial shift count as a 2s complement 6-bit number. The time is 0.1 n + 1.6 μsec, where n is the number of steps in the shift counter or the number required to effect normalization, whichever is less.
9,10,11	111	Accumulator left shift. Causes the AC to be shifted left the number of times specified in the shift count. AC bit 17 is filled by the link, but the link is unchanged. The time is 0.1 n + 1.6 μsec, where n is the step count.
12-17		Specify the step count except in the case of the setup command, which does not change the step counter.
15	1	On the setup command only, causes the MQ to be complemented.
16	1	On the setup command only, causes the MQ to be inclusive ORed with the AC and the result placed in AC. (If the AC has been cleared, this will place the MQ into the AC).

TABLE 4-2 EAE BIT ASSIGNMENTS AND OPERATIONS (Continued)

Bit Positions	Bits	Function
17	1	On the setup command only, causes the AC to be inclusive ORed with the SC and the results placed in AC bits 12-17. (If the AC has been cleared, this will place the SC into the AC).

TABLE 4-3 EAE INSTRUCTIONS

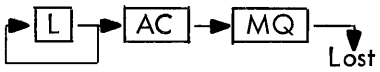
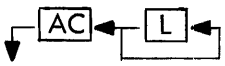
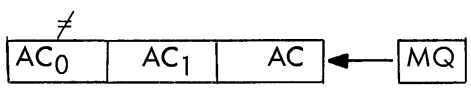
Mnemonic Symbol	Octal Code	Operation	Cycle Time (Approximate)
EAE	640000	Basic EAE command. Acts as NOP instruction. Delays program 1 cycle.	1.5 μsec
LRS	640500+n	Long right shift. Shifts the contents of the AC and MQ right the number of positions indicated in 00+n where n = number of shifts. 	1.5 μsec +0.5 μsec per shift
LRSS	660500+n	Long right shift, signed. Shifts the contents of the AC and MQ the number of positions indicated in 00+n. The contents of AC_0 are initially duplicated in the link. During shifting, the contents of the link fill AC_0. $AC_0 \rightarrow$ LINK 	1.5 μsec +0.5 μsec per shift
ALSS	660700+n	Accumulator left shift, signed. Shifts the AC left the number of positions indicated in 00+n. The contents of AC_0 are initially duplicated in the link. During shifting, the contents of the link fill AC_{17} and 	1.5 μsec +0.5 μsec per shift
NORM	640444	Normalize, unsigned. The contents of the AC and MQ are shifted left until the contents of bit AC_0 are not equal to bit AC, ($AC_0 \neq AC_1$) or until the contents of the AC and MQ are shifted left 36 times (44_8). 	1.5 μsec +0.5 μsec per shift

TABLE 4-3 EAE INSTRUCTIONS (Continued)

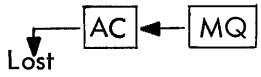
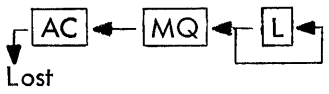
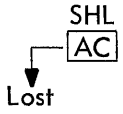
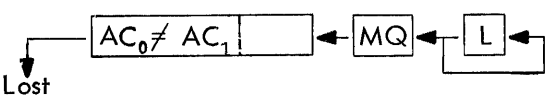
Mnemonic Symbol	Octal Code	Operation	Cycle Time (Approximate)
LLS	660500+n	Long left shift. Shift the contents of the AC and MQ left the number of positions indicated in +n. 	1.5 μsec +0.5 μsec per shift
LLSS	660600+n	Long left shift, signed. Shifts the contents of the AC and MQ left the number of positions indicated in +n. The contents of AC_0 are initially duplicated in the link. During shifting, the contents of the link fill MQ_{12} and remain unchanged. $AC_0 \rightarrow LINK$ 	1.5 μsec +0.5 μsec per shift
ALS	640700+n	Accumulator left shift. Shifts the contents of the AC left the number of positions indicated in +n. 	1.5 μsec +0.5 μsec per shift
NORMS	660444	Normalize, signed. This instruction is used as part of the subroutine to convert an integer into a fraction, and an exponent for use in floating point arithmetic. The contents of AC_0 are duplicated in the link. The contents of the AC and the MQ are shifted left by this command until $AC_0 \neq AC_1$ or until the contents of the AC and MQ shift 36 times (44_8). The link fills MQ_{17} and remains unchanged. $AC_0 = LINK$ 	1.5 μsec +0.5 μsec per shift

TABLE 4-3 EAE INSTRUCTIONS (Continued)

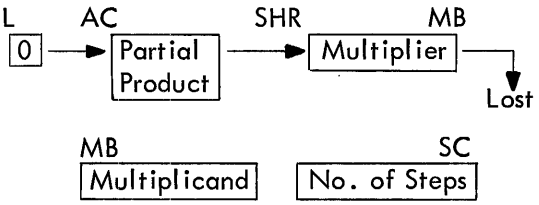
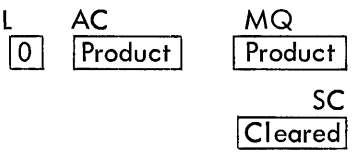
Mnemonic Symbol	Octal Code	Operation	Cycle Time (Approximate)
MUL	653122	Multiply, unsigned. This instruction multiplies two 18-bit unsigned numbers to form a 36-bit product. The multiplier is loaded into the MQ by this instruction. $0 \rightarrow MQ$ $AC \vee MQ$ The AC is cleared. $0 \rightarrow AC$ The 2s complement of the number of bits in the multiplier is transferred to the SC, $\overline{MB_{12} \rightarrow MB_{12}} \rightarrow SC$ and the unsigned multiplicand is in location Y+1. This instruction stops the computer timing cycle during the fetch cycle of Y+1 (multiplicand in the MB). Multiplication begins with the CPTC stopped with the major register as follows:  On completion of multiplication the major registers are as follows: 	
MULS	657122	This instruction multiplies two 17-bit signed numbers to form a 34-bit double signed product. This instruction is microcoded to perform the following: 1) Clear the MQ $0 \rightarrow MQ$ 2) Get sign of multiplier $AC_0 \rightarrow$ EAE AC sign register	

TABLE 4-3 EAE INSTRUCTIONS (Continued)

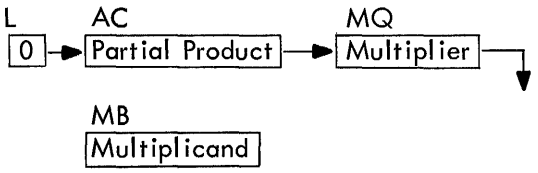
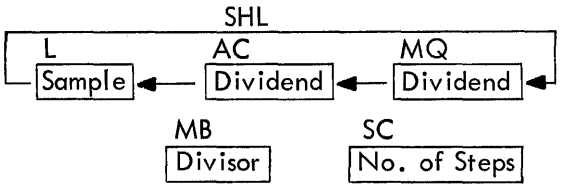
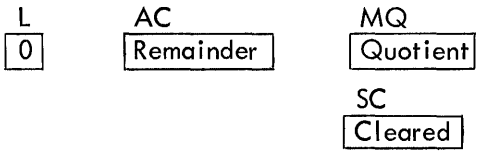
Mnemonic Symbol	Octal Code	Operation	Cycle Time (Approximate)
		3) Transfer the multiplier from AC to MQ. AC V MQ 0 → AC 4) If sign is negative (EAE AC sign = 1) complement the MQ $(\overline{MQ} \rightarrow MQ)$ 5) Place the number of steps in SC $\overline{MB_{12}\text{-}MB_{17}} \rightarrow SC_{12}\text{-}SC_{17}$ Multiplication begins with the computer timing chain stopped. The registers are as follows: 	
DIV	640323	This instruction divides an 18-bit unsigned number at location Y+1 (divisor), into a 36-bit unsigned number (dividend) contained in the AC and MQ. The number of steps (23_8) are transferred to the SC by this instruction. Divisions begin with the major registers as follows:  At divide end, the major registers are as follows: 	

TABLE 4-3 EAE INSTRUCTIONS (Continued)

Mnemonic Symbol	Octal Code	Operation	Cycle Time (Approximate)
LACQ	641002	Places the contents of the MQ into the AC. $0 \rightarrow AC$ MQ V AC	1.6 μsec
LACS	641001	Places the contents of the SC into AC_{12}-AC_{17}. Used as part of converting an integer to a floating point number. Effectively, transfers the value of the exponent to the AC. $0 \rightarrow AC$ SC V AC_{12}-AC_{17}	1.6 μsec
CLQ	650000	Clears MQ $0 \rightarrow MQ$	1.6 μsec
ABS	644000	Duplicates the contents AC_0 in the EAE AC sign register. If EAE AC sign = 1 the AC is complemented.	1.6 μsec
GSM	664000	Get sign and magnitude, thus setting up divisor or multiplicand. Places AC sign in the link and takes the absolute value of AC.	1.5 μsec

4.3.3.2 EAE Major Units - The EAE major units are shown in figure 4-3. Refer to drawings BS-D-177-0-4 through 8.

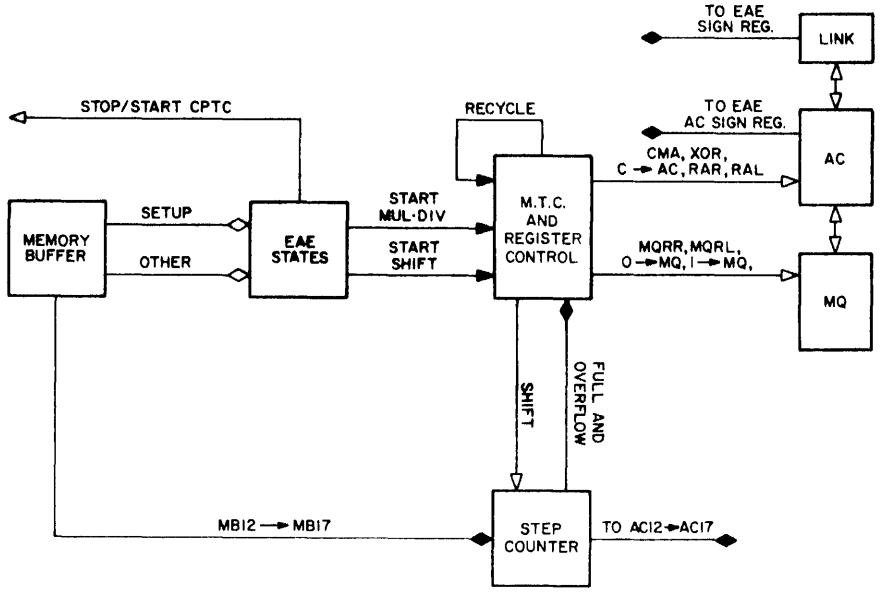


Figure 4-3 EAE Block Diagram

a. EAE States (4)

The EAE states logic decodes the command portion of the EAE instruction to determine the selected EAE state. It also contains the logic for stopping and starting the CPTC, and the logic for operating the EAE asynchronous to the CPTC. The two EAE sign registers (EAE AC sign and EAE sign) form part of this logic.

For setup instructions gate (D21, 4) decodes MB9(0), MB10(0), and MB11(0) to generate a SETUP level at gate (D20, 4). For multiplication, gate (B24, 4) decodes MB9(0), MB10(0), and MB11(1) at EAE T5 time to set the MUL flip-flop to 1.

For division, gate (D24, 4) decodes MB9(0) and MB10(1) at EAE T5 time to set the DIV flip-flop to 1.

For all shift operations gate (D17, 4) decodes the IA3(1), IB1(1), and the MUL(0) and DIV(0) levels to set the EAE·F flip-flop to 1. All shift operations start at T6 of the first EAE fetch cycle when the START SHIFT pulse is generated at gate (D24, 4).

b. Step Counter and Control (5)

The step counter (SC) is comprised of six Type B201 Flip-Flops connected as a 2-stage 6-bit octal counter. Bit registers SC15 through SC17 count the least significant octal number, and SC12 through SC14 count the most significant octal number. The count loaded

the SC determines the number of steps to be performed during the EAE arithmetic operations. The SC is loaded with the selected count during time EAE T3 of any arithmetic instruction by the BM → SC pulse developed at PA (D6,5). Because the SC is an "up" counter, the complement of the count contained in bits 12 through 17 of the arithmetic instruction is stored in the SC. (MB12 through MB17 are complement connected to SC12 through SC17).

The counting sequence starts when the INPUT (LOW COUNT) signal develops the LOW COUNT signal at PA (C19,5). The LOW COUNT signal originates at PA (B25,4) when the START MUL·DIV or the START SHIFT pulse is developed. The SHIFT pulse developed at PA (C19,5) initiates all further counts. The LOW COUNT pulse samples all input gates of SC15 through SC17 which increases the count by 1. The LOW COUNT signal also samples the status of SC15 through SC17 for 1s at gate (B23,5). If SC15 through SC17 are 1s, the HIGH COUNT pulse developed at PA (D14,5) increments SC12 through SC14 by one count. The SC FULL flip-flop is set to 1 by two methods. At EAE T5 time, gate (D26,5) is sampled. If SC12 through SC17 are 1, the FULL flip-flop is set. The other method is used with the CPTC stopped. When SC12 through SC16 are 1, gate (B24,5) develops a FILL pulse which is delayed by delay (D30,5). The FILL pulse then sets the FULL flip-flop to 1. The SCOV flip-flop sets on the shift pulse which stops all EAE operations.

c. EAE Register Controls (6)

The EAE register control contains the logic for manipulating the AC, MQ and link during EAE operations. The EAE register control also contains the adder/subtractor logic used in the multiply and divide operations. The following is a list of the control signals and their functions:

Signal	Function
CLR LINK	Clears the link at the start of the multiplication and division operation or during microprogramming if AC0 is 0
SET LINK	Sets the link to 1 during microprogramming
CMA	Complements AC
CLA	Clears AC
CML	Complements link
0 → MQ	Clears MQ
MQ RR	Rotates MQ right
MQ RL	Rotates MQ left
AC1 → MQ	Sets MQ bits to 1 which correspond to AC1 bits

Signal	Function
MQ1→ AC	Sets AC bits to 1 which correspond to MQ1 bits
XOR	Exclusive ORs the MB into the AC
CRY	Generates AC carries

d. Main Timing Chain (7)

The EAE main timing chain controls the EAE timing when the CPTC is stopped. The CPTC stops for all EAE multiply, divide, shift, and normalize operations. The EAE timing then becomes a function of the sampling and shift rates of the AC and MQ as controlled by the main timing chains.

During multiplication, the first sample is initiated by the START and SCOV(0) levels at gate B29. At T2 time gate D28 is sampled to determine if the first operation is in ADD or a SHIFT by sampling MQ17. Bit MQ16 is used for all further samples. At the end of multiplication the sign of the product is tested at gate D26. If the EAE SIGN is a 1 (the product is negative), the AC and the MQ are complemented by the CMA, 1→MQ and 0→MQ signals developed at gates D9, and C22.

For division, the first step is always subtract. The SUB flip-flop is set to 1 at EAE T2. For all other steps, the link is sampled.

e. Multiplier Quotient Register (8)

The multiplier quotient register (MQ) is comprised of 18 Type B201 Flip-Flop modules and additional B105 Gating Circuits. For multiplication, the MQ initially contains the multiplier. At the conclusion of the multiplication operation the MQ contains the least significant part of the product with the most significant part in the AC. For division the MQ initially contains the least significant part of the dividend. At the conclusion of the division operation the MQ contains the quotient with the remainder in the AC. For normalize operations, once the number normalizes, the least significant part of the number forms in the MQ. Information transfers from and to the MQ by the following methods:

(1) For EAE setup commands, the contents of the AC transfer into the MQ by the AC1→ MQ pulse gating the ACB levels into the MQ.

(2) As part of the division, normalize, and shift-left operations the contents of the MQ shift left by the MQRL (MQ rotate left) pulse gating the higher (positional) but lower (in magnitude) MQ bit into the more significant (in magnitude) MQ bit register.

(3) As part of the multiplication and shift right operations, the MQ shifts right by the MQRR (MQ rotate right) pulse gating the lower (positional) but higher (in magnitude) MQ bits into the lesser significant (in magnitude) MQ bit register.

(4) As part of the division operation, (MQ→$\overline{MQ}$), the contents of the MQ are complemented by coincidently applying the 0→MQ and the 1→MQ pulse to the MQ. The 0→MQ pulse when used alone clears the MQ, and the 1→MQ pulse places all 1s in the MQ.

4.3.3.3 Multiply - The algorithm for multiplication using the PDP-7 EAE is to sample each bit of the multiplier starting with the least significant bit and ending with the most significant bit. In the first step, the least significant bit is sampled. If it contains 1, the multiplicand is added to the partial product. If it contains 0, no action occurs. The second and all succeeding steps occur with the bit located in the next-to-least significant position which is, after the first step, the present least significant bit. If its contents are 1, the partial product is added to the multiplicand; then the partial product and the multiplier are shifted right with the contents of the least significant bit being lost. If its contents are 0, the partial product and the multiplier are shifted right. Multiplication is complete when all multiplier bits are sampled.

In the EAE, the multiplier is stored in the MQ, the multiplicand is stored in the MB, and the partial product is developed in the AC and the MQ. For the first multiplication step, the contents of MQ17 are sampled. For all succeeding steps, the contents of MQ16 are sampled. The 2s complement of the number of multiplication steps is stored in the SC. Multiplication is complete when the SC overflows.

The EAE performs multiplication at high speeds. This is accomplished by stopping the computer timing chain which allows the timing to be controlled by the sampling and shifting rates of the internal logic. Further speed is gained by sampling MQ16 after the first step. This method effectively eliminates one shift operation.

a. Sample Program

This sample program multiplies 5_8 by 2_8 as signed numbers. The two EAE instructions in this listing are:

```
ST,     0200    200100      LAC CAND        /LOAD MULTIPLIER
        0201    100500      JMS MPY         /LOCATE MULTIPLY SUBROUTINE
        0202    200101      LAC PLIER       /LOAD MULTIPLIER
        0203    740040      HLT
```

```
MPY     0500    000202      PC
        0501    664000      GSM             /GET SIGN MULTIPLICAND
        0502    040505      DAC .+3         /DEPOSIT MULTIPLICAND IN CAND
        0503    400500      XCT I MPY       /LOAD MULTIPLIER
        0504    657104      MULS            /SHIFT 4 TIMES AC → MQ, 0 → AC
CAND    0505    000003      MULTIPLICAND
        0506    440500      ISZ PC
        0507    620500      JMP I 500       /JUMP TO MAIN PROGRAM

        0100    000002      MULTIPLICAND
        0101    000005      MULTIPLIER
```

This program uses 4-bit registers.

```
 0010      MULTIPLICAND
 0101      MULTIPLIER
 0010      PARTIAL PRODUCT
0100

01010      PRODUCT
  12(8)
```

The setup instruction 664000 GSM is used in EAE signed multiply operations to place the sign of the multiplicand in the link with the AC contain the absolute value of the multiplicand. This operation is required before transferring AC → MB. During the execution of GSM, a fetch cycle is initiated. The PC increments by 1; the MA contains the contents of PC before incrementation. The MB contains the GSM instruction, and the AC contains the signed multiplicand.

MB ← REGISTER $(664000)_8$

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
1	1	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0

← EAE → Instruction

AC0 → LINK

AC0 → EAE AC SIGN

EAE ← SETUP →

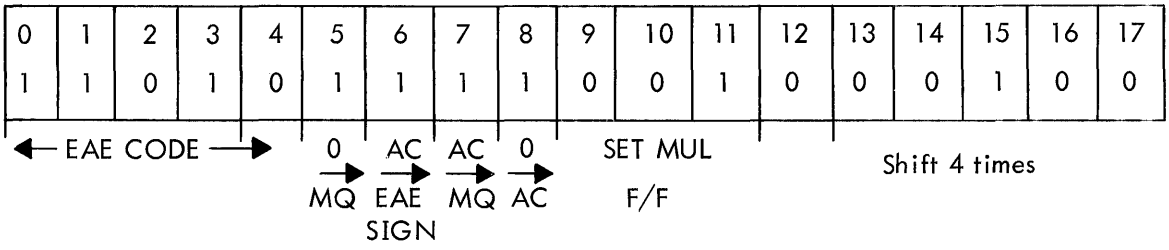
The EAE events during the fetch cycle are (see EAE flow diagram FD-177-0-2):

EAE Flow

	T1	NO EAE EVENTS
	T2	1→ EAE·F (IR decoded)
EAE T1	T3	0→STOP SHIFT, 0→ADD, 0→SUB
		MB4(1) = AC0→ LINK (places multiplicand sign into link)
		MB6(1) = AC0→EAE AC SIGN
		MB9, 10 , 11(0) = EAE SETUP
	T4	NO EAE EVENTS
	T5	EAE AC SIGN ⊻ LINK→ EAE SIGN
	T6	NO EAE EVENTS
	T7	EAE SETUP = CLR→EAE SIGN, EAE AC SIGN CLR SIGN, MUL, DIV, SCOV, FULL, and NORM

At the conclusion of this instruction the AC contains the absolute value of the multiplicand, and the link contains the multiplicand sign.

MULS 65 7104, AC→MQ, 0→AC



EAE Flow (Fetch Cycle)

	T1	NO EAE EVENTS
	T2	1→EAE·F F/F
	T3	0→STOP SHIFT F/F
		0→ADD F/F
		0→SUB F/F
		OTHER = $\overline{\text{MB12-17}}$ ↓ SC12-17
	T4	AC1→MQ (multiplier) MQ
		0→AC

T5	MB9(0)·MB10(0)·MB11(1)=1 MUL F/F
	MUL=1=INHIBIT BREAK REQUEST
	EAE AC SIGN ⊻ LINK →EAE SIGN
T6	NO EAE EVENTS
T7	SET NORM F/F

The multiplier is in the MQ, and the sign of the product is in the EAE sign register. The next instruction fetched contains the multiplicand, and an argument fetch cycle is initiated.

	CP	EAE
	FETCH ~	
T1	0→IR, PC-IM	NO EAE EVENTS
	+1→PC	
T2	0→MB	0→EAE·F, MUL·MQ17(1) = 1→ STOP F/F
T3	SAI→MB	START MUL·DIV,
	DZM→IR	DZM→ IR
	FORCE "B" SET	FORCE "E" SET
T4	E ~	
	AND	
	STOP	
	CPTC	

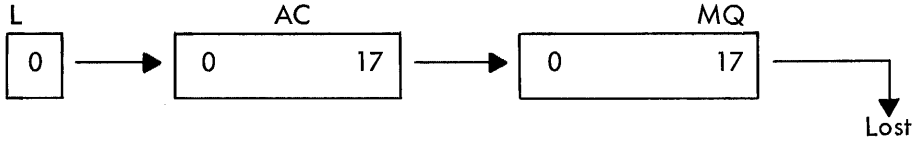
At the conclusion of this instruction the MB contains the multiplicand and (2_8), the accumulator = 0, and the multiplier (5_8) is in the MQ. The INPUT LOW COUNT increments the SC by 1 which starts the multiplication operation.

b. Example - Multiply $2_8 \times 5_8$

With the CPTC stopped, the timing is controlled by the EAE shifting and sampling rates. The initial condition of the registers are as follows: 4-bit AC and MQ registers are used for the purpose of explanation.

MB (Multiplicand)	Link (Sign)	AC (Product)	MQ (Multiplier)
0010	0	0000	0101

All shifts are to the right, with the link



The SC is preset by MULS as follows:

$$111\ 011 = -4$$

The START MUL DIV pulse initiates the INPUT LOW COUNT which increments the SC by 1 and samples MQ17 for a 1. Sampling occurs before shifting except for the initial MQ17 sample. For all further operations, the CPTC is stopped and MQ16 is sampled.

MULS $5_8 \times 2_8$ (4-Bit Registers)

Multiplicand (MQ)	Link	Product (AC)	Multiplier (MQ)
0010	0	0000	0101
		Add 0010	
	0	0010	0101 ↑ Sample
Setp 1	SHR 0	0001	0010
0010	0	0001	0010 ↑ Sample
Step 2	SHR 0	0000	1001
0010	0	0000	0110
		Add 0010	
		0010	1001 ↑ Sample
Step 3	SHR 0	0001	0101
0010	0	0001	0100
	SHR 0	0000	1010
Step 4	Answer = 12_8		
	Remember to look back at MQ16 before shifting MQ16(1) ADD then shift		

STEP COUNTER						
12	13	14	15	16	17	
1	1	1	0	1	1	4
1	1	1	1	0	0	Input Low Count
1	1	1	1	0	1	1st Shift
1	1	1	1	1	0	2nd Shift
1	1	1	1	1	1	3rd Shift
0	0	0	0	0	0	4th Shift

Note: The timing chain starts when the operation has been completed.

c. Block Logic Discussion

This description is the detailed discussion of the functional operation of the EAE logic elements during the execution of the MULS instruction 657104_8. Refer to drawings BS-D-177-0-4 through 7.

At T1 of the fetch cycle, the MULS instruction is fetched from memory and placed in the MB.

At T2, the IR decodes bits 0-3 to produce the IA3 and IB1 levels (OP code 64). These levels coincide with the 0 states of the MUL and DIV flip-flops (C24,4) condition NAND gate (D17,4) to set the EAE·F flip-flop to a 1.

At T3, the EAE T3 pulse developed at inverter (C31,7) clears the STOP SHIFT, ADD, and SUB flip-flops (C26,7) to 0. Also, the MB→SC developed at PA(C11,5) transfers the complements of MB bits 12-17 (111011) to the step counter, SC12-17, (C14-C18,5). The 0→MQ signal developed at PA(A23,6) clears the contents of the MQ to 0, and MB5 is a 1.

At T4, the AC→MQ signal developed at PA(C11,6) transfers the contents of the AC to the MQ. MB8 is a 1, and the CLA pulse developed at inverter (D10,6) clears the AC to 0.

At T5, the EAE T5 signal combined with the MB9(0), MB10(0), and MB11(1) levels conditions NAND gate (B24,4) to set the MUL flip-flop (C24) to a 1. The MUL 1 level generates a MUL·DIV level at NOR gate (D23,4). This level is applied to the central processor interrupt control logic to prevent a break request from interrupting the EAE operations. Also, at T5, the EAE T5 level samples the status of the link and the EAE AC sign register for a 1 condition at NAND gates (D25,4). If a 1 condition is sensed, the EAE sign register is set to a 1.

At T6 no EAE events occur.

At T7, the T7 signal combines with the EAE·F level to set the NORM flip-flop (C25,5) to a 1.

At the conclusion of the fetch cycle, the multiplier is in the MQ, the AC is cleared, and the sign of the product is in the EAE sign register. As indicated in the sample program, the program proceeds to the next instruction which contains the multiplicand, thus initiating another fetch cycle. At T1, the normal fetch cycle operations occur: The OP code 0_8 is decoded in the IR, the contents of the PC are transferred to the MA, and the PC is incremented by 1.

At T2, the T2 signal clears the EAE flip-flop to 0 and also samples the status of MUL and MQ17 for a 1. Since the MUL flip-flop was set to a 1 in the previous fetch cycle and MQ17 is a 1, NAND gates (D27,7) condition the STOP SHIFT and ADD flip-flops (C26,7) to the 1 state.

At T3, the T3 signal enables NAND gate (D23,4) which developes the START MUL·DIV signal at PA (C23,4). The START·MUL signal triggers the delay (D19,4) which generates three signals at PA (B25,4):

(1) The INPUT LOW COUNT which increments the step counter (SC)

(2) The STOP CPTC pulse which stops the computer timing chains, and

(3) The START pulse which starts the multiplication operation asynchronous to the CP timing chain.

The START·MUL·DIV signal also generates the CLEAR LINK signal at PA(C3,6). The START pulse combined with the SCOV(0) level conditions NAND gate (B29,7) to sample the states of the ADD and STOP SHIFT flip-flops at inverters (B29,7). Since both flip-flops are a 1 (at T2), the RECYCLE signal is temporarily inhibited and an ADD signal is generated.

d. Adder Operation During Multiply

The ADD pulse generated in inverter (B29,7) develops an XOR pulse at PA(A28,6). The XOR performs MB ∀ AC → AC which effectively half adds the MB with the AC. The ADD pulse, delayed 100 μsec at delay (A28,6), generates an AC CARRY pulse completing the addition of the MB into the AC. The delayed ADD pulse also develops a RESET pulse at inverter (C31,6) which clears the ADD and STOP SHIFT flip-flops. When the AC CARRYS are complete, the CP generates a CRY DET signal. This signal gates inverters (B28,6) which generate a RECYCLE pulse. The associated logic at B27 and C25 applies only to the adder divide routine. The RECYCLE pulse at PA(B30,7) generates a SHIFT pulse which shifts the AC and MQ right one position by the MQRT signal and RAR signal developed at gates (C20,7).

In summary, the above adder sequence completes the initial multiplication step which originated at T2 when MQ17 was sampled. For all further operations MQ16 is sampled at gates (C29,7). If MQ16 is a 0, neither the STOP SHIFT nor the ADD is set to a 1, and a shift operation occurs. If MQ16 is a 1, both flip-flops are set to a 1, and an ADD operation occurs followed by a shift.

4.3.3.4 Divide - The algorithm for division is to subtract and shift left. Division begins with the divisor in the MB, and the dividend in the MQ. The dividend is subtracted from the divisor. If the result is a positive number, a 1 is placed in the quotient. If the result is a negative number, a 0 is placed in the quotient. If the result of the first subtraction is a positive number, divide overflow occurs which stops the divide operation. If the result of the subtraction is a positive number in any cycle but the first, the dividend is rotated one place to the left with respect to the divisor and the operation continues with another subtraction. A subtraction with a negative number resulting is followed by an addition. The dividend is then rotated one position to the left and the subtraction is repeated to determine the next bit of the quotient. At completion of the operation the quotient is in the MQ and the remainder in the AC. For the EAE, the link is sampled.

a. Sample Program

The program listing contains two EAE instructions, a setup instruction

0501-673000/LMQ

and the arithmetic instruction

0203-645306/DIVS

This program initially loads the dividend into the AC (LAC). The contents of the AC are transferred to the MQ (LMQ) and the sign of the dividend is tested. If the sign is negative, the link is set to 1. The divisor is fetched from memory and loaded into the AC (JMS and LAC), then placed back in memory at the location DIVL. DIVL is the location of the instruction to be performed immediately following the EAE arithmetic instruction DIVS. Thus the divisor is in the MB during the execute cycle of the DIVS instruction.

Sample Division Routine

$(12_8 \div 5_8 = 2_8)$

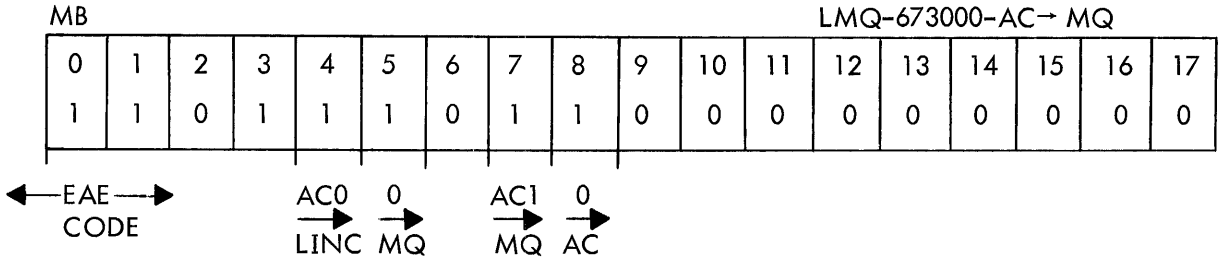
(1) MB Divisor 5_8 MQ Dividend 12_8

(2) AC REMAINDER MQ QUOTIENT

```
ST,     0500    200100      LAC DIVIDEND    /LOAD DIVIDEND
        0501    673000      LMQ             /TRANSFER TO MQ
        0502    100200      JMS DIV
        0503    200101      LAC DIVISOR     /LOAD DIVISOR
DIV,    0200    000503                      /STORE ADDRESS OF DIVISOR
        0201    420200      XCT I DIV
        0202    040204      DAC IN DIVL
        0203    645306      DIVS,
```

DIVL,	0204	000005	DIVISOR
	0205	440200	INCREMENT STORED PC
	0206	620200	EXIT SUBROUTINE
	0100	000012	DIVIDEND
	0101	000005	DIVISOR

Divide Setup Instruction



The contents of the AC are transferred to the MQ.

EAE Flow

T1 NO EAE EVENTS

T2 1→ EAE·F F/F

T3 0 STOP SHIFT, ADD, SUB F/Fs

MB4(1) = SIGN OF DIVIDEND TO LINK

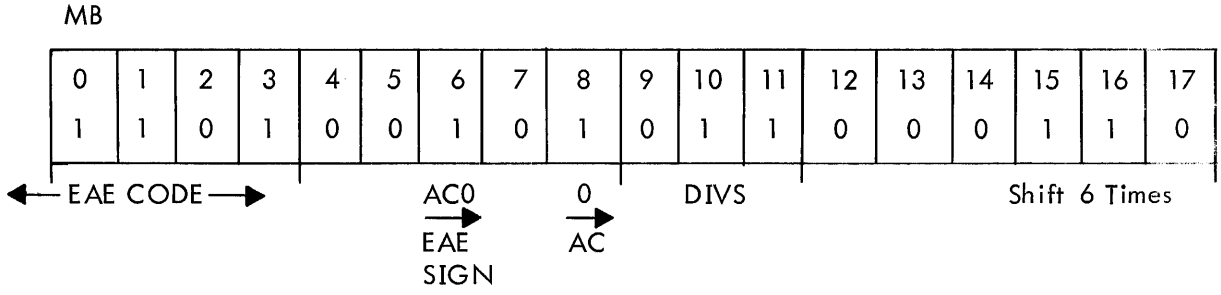
MB5(1) = 0→ MQ

MB9, 10, 11 = 0→SETUP

T4 MB7(1) = AC1s→ MQ

MB8(1) = 0→ AC

At completion of this instruction, the sign of the dividend is in the link, the dividend is transferred to the MQ, and the AC is cleared.



EAE Flow

T1 NO EAE EVENTS

T2 1 → EAE·F

T3 0 → STOP SHIFT, 0 → ADD, 0 → SUB
MB6(1) AC0 → EAE AC SIGN
(check sign of divisor)
SETUP = MB12-17 → SC
(initialize step counter)

T4 0 → AC

T5 MB9(0)·MB10(1): 1 → DIV, 1 → DIV 1st.
MUL, DIV· = INHIBIT BREAK REQUEST
EAE AC SIGN ⊻ LINK → EAE SIGN
(will answer be negative)

T6 NO EAE EVENTS

T7 1 NORM

The final results are: AC equals 0; the divisor is in location following instruction DIVS; the dividend is located in the MQ; and the EAE AC sign holds the SIGN.

EAE Flow

T1

T2 0 → EAE·F, DIV(1) 1 → SUB, 1 → STOP SHIFT

T3 MUL V DIV: START MUL, DIV,
0 → L, DZM → IR, FORCE E SET

T4 Now in execute cycle,

T5 timing chain stops at T7, MS

T6 indicates BVF

T7

Final Results

(1) All registers have been set up

Divisor	Sample	Remainder	Dividend
MB	L	AC	MQ
00101	0	00000	01010

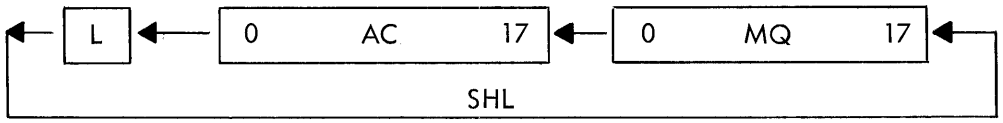
(2) If the link is a 0, subtract, then shift left.

(3) If the link is a 1, add, then shift left.

(4) Always sample the link before shifting.

(5) On the first divide the MB must be greater than the AC.

*Registers



STEP COUNTER

	12	13	14	15	16	17	
	1	1	1	0	0	1	−6
	1	1	1	0	1	0	Input Low Count
	1	1	1	0	1	1	1st Shift
	1	1	1	1	0	0	2nd Shift
	1	1	1	1	0	1	3rd Shift
	1	1	1	1	1	0	4th Shift
MQ Left	1	1	1	1	1	1	5th Shift
Only	0	0	0	0	0	0	6th Shift

Example $12_8 \div 5_8 = 2_8$

Divisor	Link	Accumulator		Dividend
MB	L	AC		MQ
00101	0		00000	01010
	CML 1	CMA	11111	01010
		Add	00101	
1st divide, sample link,	CML 0	AC0 CRY	00100	
sample link before shift,	CML 1	CMA	11011	01010
00101	SHL 1		10110	10101
	Note: AC0 CRY = CML			
Step 1				
00101	1		10110	10101
		Add	00101	
Sample link	1		11011	10101
Shift left	1		10111	01011

*Five-bit register for explanation only.

Divisor	Link	Accumulator		Dividend
Step 2				
00101	1		10111	01011
		Add	00101	
Sample link	1		11100	01011
Shift left	1		11000	10111
Step 3				
00101	1		11000	10111
	1	Add	00101	
Sample link	1		11101	10111
Shift left	1		11011	01111
Step 4				
00101	1		11011	01111
	1	Add	00101	
Sample link	CML 0	AC0 CRY	00000	01111
Shift left	0		00000	11110
Step 5				
MB	L	AC		MQ
00101	0		00000	11110
Subtract	CML 1	CMA	11111	
	1	Add	00101	
	CML 0	AC0 CRY	00100	
Sample link	CML 1	CMA	11011	11110
Shift left				
MQ only				
FULL (1)	1		11011	11101
Last ADD	1		00101	
	CML 0	AC0 CRY	00000	11101
	Function Complete	Complement MQ		
	0		00000	00010
	L	REMAINDER		QUOTIENT

Start central processor time chain and complete rest of program.

b. Logic Block Discussion

This description is the detailed discussion of the functional operation of the EAE logic elements during the execution of the DIVS instruction 645306.

At T1 of the fetch cycle, the DIVS instruction is fetched from memory and placed in the MB.

At T2, MB bits 0 through 3 are decoded in the IR to produce the IA3 and IB1 levels. These levels, coincident with the 0 states of the DIV flip-flop (C24, 4), condition NAND gate (D17, 4) to set EAE·F flip-flop to 1.

At T3, the EAE T3 timing pulse clears the STOP SHIFT, ADD, and SUB flip-flops to 0. Also at T3, if AC0 is a 1 and MB6 is a 1, NAND gate output (D25, 4) sets EAE AC SIGN register to 1. (The sign of the quotient is in the EAE sign register.) The contents of $\overline{MB12\text{-}17}$ are transferred to SC11-17 by the MB →SC signal generated at PA (D13, 5).

At T4, when MB8=1, the CLA pulse developed at inverter (D16, 6) clears the AC.

At T5, the EAE T5 pulse with the MB9(0) and MB10(0) levels conditions NAND gate (D24, 4) set the DIV flip-flop (C24, 4) to 1. The 1 level of the DIV flip-flop (C24, 4) sets the DIV FIRST flip-flop (C14, 7) to a 1. Also at T5, the EAE sign register (C24, 4) is set to 1 if either the link or the EAE AC sign is a 1.

At T7, the NORM flip-flop is set to 1. At the conclusion of the DIVS instruction, the AC is cleared, the divisor is in the location following DIVS, the dividend is in the MQ, and the EAE sign register contains the sign of the quotient.

The next instruction is fetched from memory (DIVISOR) and a second fetch cycle is initiated.

At T2, the EAE·F F/F (C26, 4) is reset to 0.

At T3, a START MUL·DIV signal is generated.

c. Subtract (See figure 4-4)

The SUB signal developed at gate (B29, 7) generates the ADD 1 pulse at PA (A28, 6). The ADD 1 pulse conditions inverters (D10, 6) to produce the CMA and CML signals. These signals respectively complement the AC and the link. The ADD 1 pulse also conditions the COMP flip-flop to a 1 and delayed 100 μsec at delay (A26, 6) generates the ADD 2 pulse.

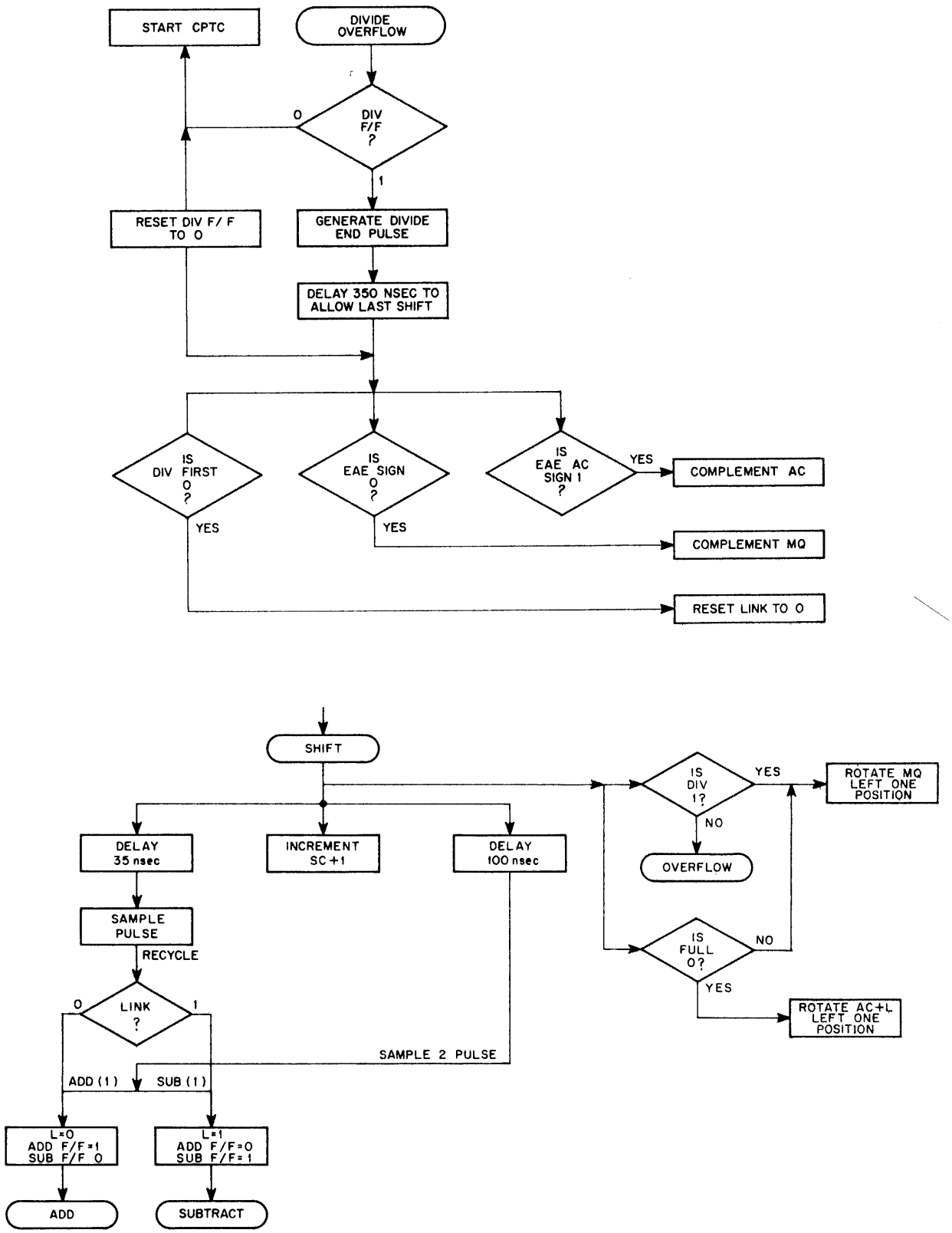


Figure 4-4 EAE Divide Flow Diagram

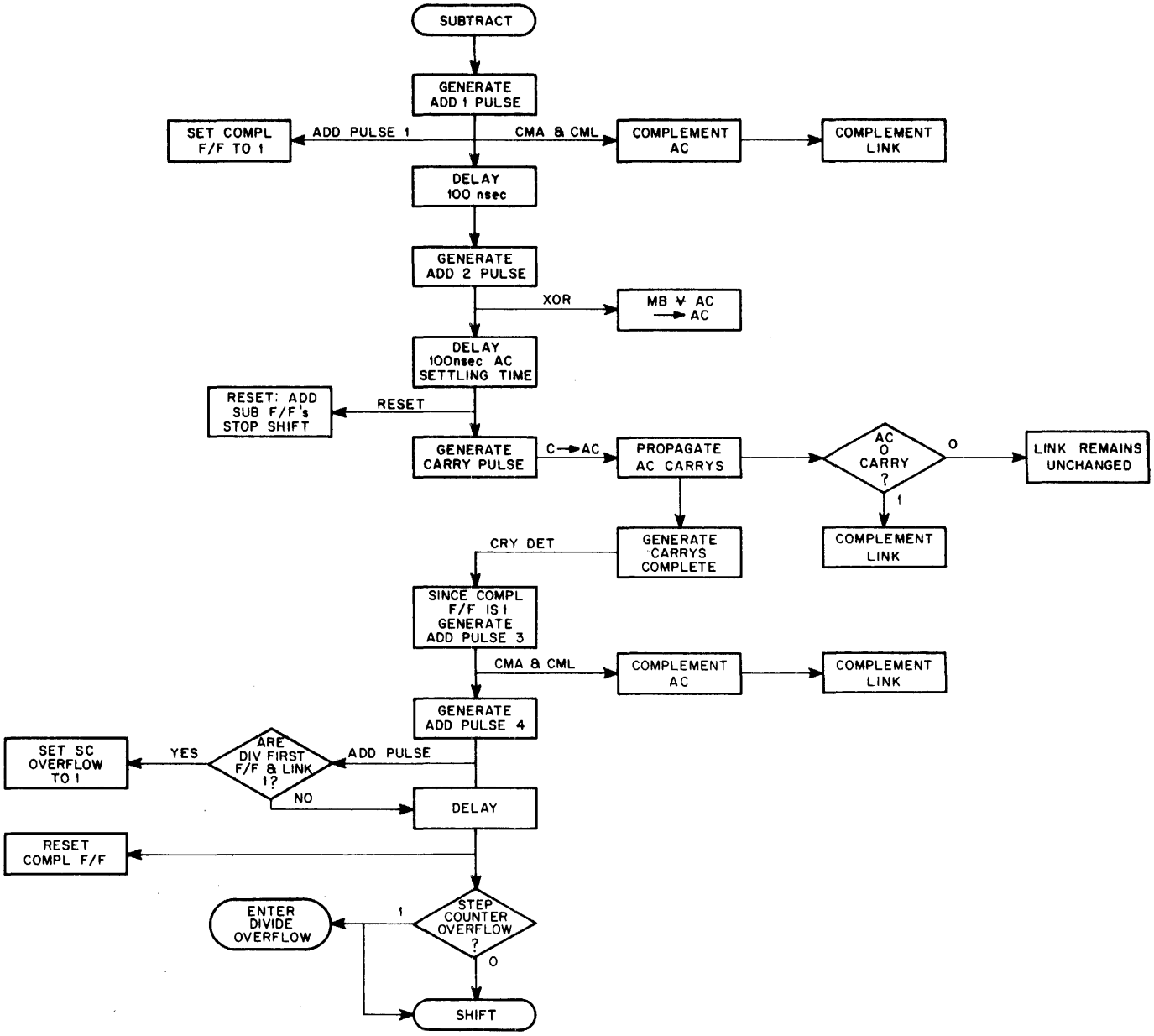


Figure 4-4 EAE Divide Flow Diagram (continued)

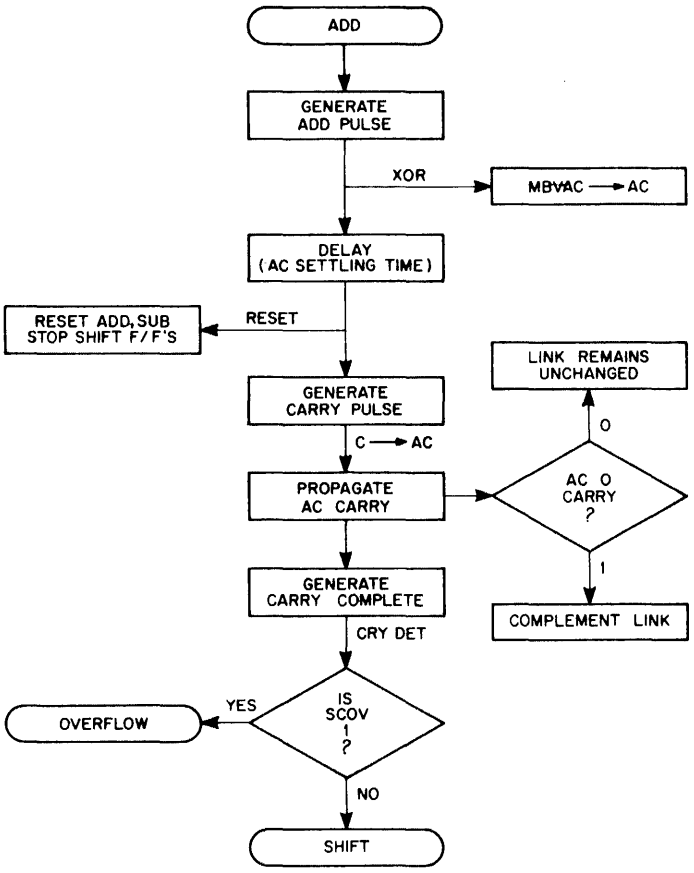


Figure 4-4 EAE Divide Flow Diagram (continued)

The ADD 2 pulse generates the XOR signal at PA(A28,5) which logically performs MB ∀ AC→ AC. The pulse delayed 100 μsec by delay (A28,6 generates the CRY which propagates AC carries. If AC0 CARRY is a 1, the link is complemented again. ADD pulse 2 also resets the ADD, SUB, and STOP SHIFT flip-flops. Once the carries are completed, the CP generates a CRY DET pulse. The CARRY DET pulse develops the ADD3 signal at PA(A27,6). This signal strobes the COMP flip-flop output gates (B28,6) to generate the CMA and CML levels at inverters (D10,6) which recomplement the AC and link and generates the ADD 4 pulse.

The ADD 4 pulse senses the status of the link and DIV 1ST flip-flop (C14,7) at NAND gate (B26,7). If the link is a 1 on the first division step, the SCOV flip-flop (C25,5) is set to 1 and the EAE divide operation stops. The CPTC starts again and the overflow condition is indicated. The ADD 4 pulse also triggers two delays (A27 and A25,6) to reset the COMP flip-flop (C25,6) and to generate the RECYCLE pulse at gate (B28,6) if the SCOV level is a 0.

In summary, if the link is a 1 when sampled, the subtract routine is initiated. The AC and L are complemented, the MB is added to the AC. If add overflow occurs, the L is complemented again. The AC and link are restored. On the first divide, the link is resampled. If it is a 1, divide overflow occurs. This indicates that if the divisor is greater than the dividend, rescaling is required.

d. Shift Divide

Once the ADD or SUB operations are complete, the RECYCLE pulse starts the SHIFT operation. The RECYCLE pulse develops the SHIFT signal at PA(B30,7). The SHIFT signal conditions gate (D23,7) to shift the AC left with the RAL pulse developed at gate (C20,7), to shift the link left with the LEFT ROTATE signal developed at gates (D9,7), and the MQ left with the MQ LFT signal developed at gate (C20,6). The SHIFT signal resets the DIV FIRST flip-flop (C14,7) to 0, and increments the SC one count at gate (D18,5). The SHIFT signal is also applied to delay (D31,7 and B30,7). Delay (D31,7) relays the SHIFT pulse 35 μsec to develop the SAMPLE pulse at PA(D31,7). The SAMPLE pulse senses the status of the link at gates (D28 and D24,7) to set either the ADD or SUB flip-flops (C26,7). Delay (B30,7) delays the SHIFT pulse 100 μsec; then strobes gates (B29,7) to initiate the next ADD or SUB operations.

e. Divide Overflow

Divide overflow occurs when the SCOV flip-flop (C25,5) sets to 1. This indicates that all division steps are complete. The OVFLO pulse conditions NAND gate (D28,7) to trigger the one-shot delay (A30,7). Delay (A30,7) produces a 350-μsec divide end pulse at PA(C23,7). The pulse strobes the following gates:

(1) Gate (D15,7) if EAE AC sign is a 1, the AC is complemented by the CMA pulse.

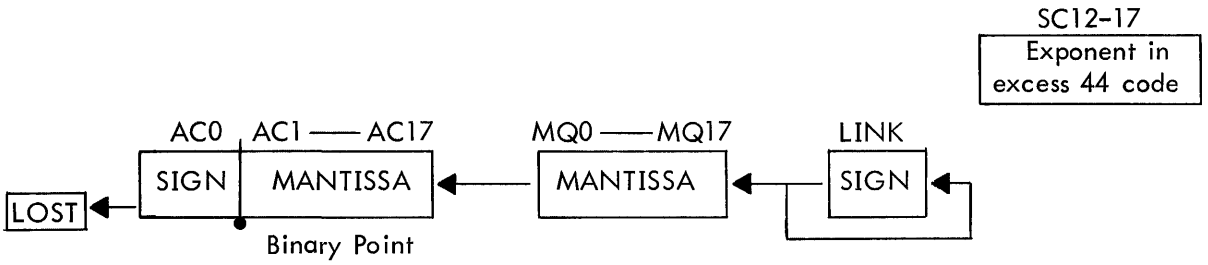
(2) Gates (A22,7) if EAE sign is a 0, the MQ is complemented by the 1→ MQ and 0→ MQ pulses.

(3) Gate (B27,7), the DIV flip-flop is reset by the 0 DIV pulse.

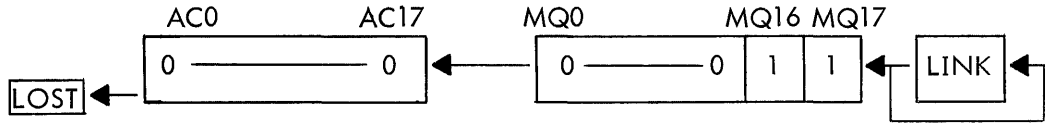
(4) Gate (D12,8) if the DIV FIRST flip-flop is 0, the link is reset by the 0 L pulse.

4.3.3.5 Normalize - This command is used as part of the conversion of an integer into a fraction and an exponent for use in floating-point arithmetic. The algorithm for normalize is to shift the AC and MQ left until the contents of AC0 do not equal the contents of AC1 (AC0 ≠ AC1). For positive numbers AC0 is (0) and AC1 is (1). For negative numbers AC0 is (1) and AC1 is (0). For signed normalized numbers (NORMS) the sign of the number is duplicated in the link. In other words, after normalization L = AC0. The link fills MQ17 and does not change.

For normalized numbers, the binary point of the fraction is assumed to be between AC0 and AC1, the mantissa of the fraction is from AC1 to MQ17, the sign in AC0, and the value of the exponent in the step counter (SC).



The number in the SC at normalization is actually the 2s complement of the exponent (– N) plus the characteristic (S). The characteristic is a number equivalent to the total number of bit positions in the AC + MQ (36_{10} or 44_8). As part of the NORMS instruction (44_8) is loaded into the SC to establish the exponent in excess 44 code. This means that the exponential range of the fraction (mantissa) is from 2^0 to 2^{35} when normalized. For example, if the integer +3 is stored in bits MQ16 and MQ17 and we wish to convert this to a fraction and exponent, the following steps are required:



a. Load a number in the SC equal to the maximum number of shifts (S) (44_8).

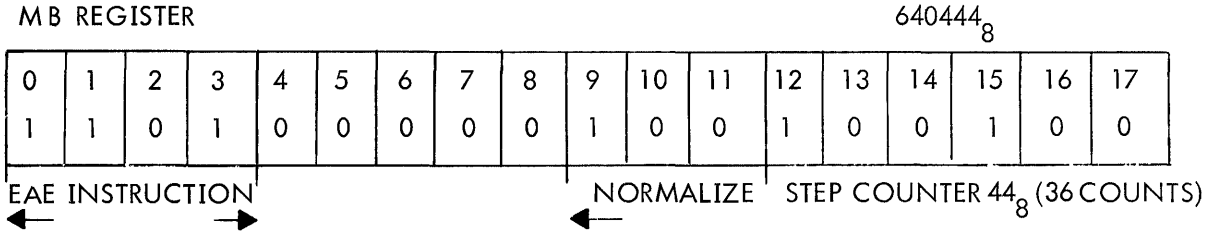
b. Place the binary point between AC0 and AC1.

c. Shift left until MQ16 is shifted into AC0.

d. Count the number of shifts performed (N).

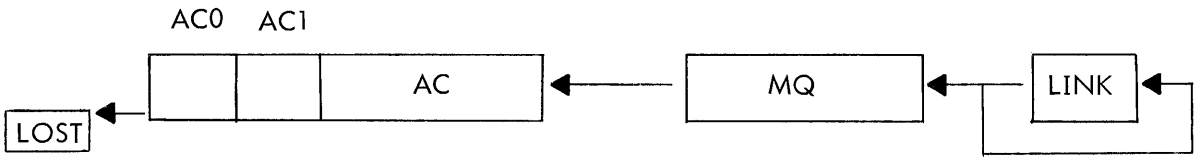
e. Subtract the characteristic (44_8) from the number of shifts performed to get the exponent of the fraction.

The number to be normalized is loaded into the AC or MQ and the NORMS instruction is fetched from memory.



EAE Flow (Fetch Cycle)

T1	NO EAE EVENTS
T2	1→EAE·F
T3	MB9(1), MB10(0), MB11(0) = OTHER
	OTHER = MB12→17
T4	NO EAE EVENTS
T5	MB8(0)·NORMALIZED = 0→FULL
T6	MB9(1) = START SHIFT
T7	SET NORM
	STOP CPTC



a. Detailed Block Diagram Discussion

At T6, the START SHIFT signal developed at NAND gate (D24,4) (EAE·F and MB9 are 1) initiates the normalize operation. The START SHIFT triggers 100-nsec delay (D19,4) which increments the SC(INPUT LOW COUNT), stops the computer timing chain (STOP CPTC), and starts the sampling operation (START pulse at NAND gate B29,7).

At T7, the NORM flip-flop (C25,5) is set to 1 and the first normalizing sample occurs at NAND gates (D16,5). If the AC is already normalized, gate (D15,5) sets the SCOV flip-flop to 1 which inhibits the START pulse at gate (B29,7) from starting the shift operation.

All shifts are to the left for normalizing. The START pulse strobes gate (B29,7). If the STOP SHIFT flip-flop is 0, a RECYCLE pulse is developed at gate (B29,7). The RECYCLE pulse developes the SHIFT pulse at PA(B30,7), and the SHIFT pulse develops the RAL signal at gate (D22, pins K and L), and the MQ LFT signal at gate (D22, pins P and N,7). The AC and MQ are shifted left one position. The SAMPLE pulse developed at delay (D21,7) senses the status of NAND gates (D29,7). If either gate is a 1, the STOP SHIFT flip-flop sets to 1 inhibiting the RECYCLE pulse from initiating another shift except the shift operation already in progress.

CHAPTER 5
MAINTENANCE

5.1 INTRODUCTION

Basically, the PDP-7 maintenance system is directed to the module-replacement level. Thus, downtime caused by malfunctions can be minimized and the system more readily kept on-line. The maintenance effort is divided into preventive and corrective catagories, for descriptive convenience.

Preventive maintenance consists of routine periodic checks such as visual inspections, standard maintenance procedures involving cleaning and lubricating, and occasional marginal-checking to expose weakening conditions before they become malfunctions. Periodic maintenance also requires use of the standard testing equipment listed in table 5-1.

When a malfuction occurs, corrective maintenance is instituted to isolate the problem and make proper adjustments or replacements. Primarily this involves the use of diagnostic routines designed to test the functional units of the system. Strictly speaking, categorizing these primary areas does not imply complete independence. The prodedures and techniques of periodic checking can aid and are indeed necessary in malfunction tracing; and conversely, intermittent error conditions occurring during system operations can be caused to occur continuously by applying marginal conditions. In this way, a proper diagnostic can then be run to isolate and identify the problem.

Diagnostic routines are provided on perforated paper tape to be mounted and executed as described in chapter 2, Operations, and documentation listed in table 1-3 of chapter 1, is provided for each available routine.

5.2 MAINTENANCE EQUIPMENT REQUIRED

Maintenance activities for the PDP-7 system require availability of the standard test equipment and special material listed in table 5-1, also standard hand tools, cleaners, test cables and probes.

TABLE 5-1 MAINTENANCE EQUIPMENT

Equipment	Manufacturer	Designation
Multimeter	Triplett or Simpson	Model 630-NA or 260
Oscilloscope	Tektronix	Type 547
Plug-in-Unit	Tektronix	Type CA
Clip-on Current Probe	Tektronix	Type P6016
X10 Probe	Tektronix	P6008
Recessed tip, 0.065 inch for wire wrap terminals	Tektronix	206-052
Current Probe Amplifier	Tektronix	Type 131
Hand Unwrapping Tool	Gardner-Denver	500130
Hand-Operated Wire-Wrap Tool with a 26263 bit for 24 AWG Wire and 18840 Sleeve	Gardner-Denver	14H1C
FLIP CHIP Module Extender*	DEC	Type W980
Paint Spray Can*	DEC	DEC Blue 5150-S65
Air Filter*	Research Products Corp.	EZ Clean 2-inch Type MV
Filter-Kote*	Research Products Corp.	By Name
	Documents and Test Tapes	
Teleprinter Input/Output Test*	DEC	Digital-7-50-M
Clock Interrupt Test Program*	DEC	Digital-7-51-M
CONTEST II*	DEC	Digital-7-52-M
Reader and Punch Test *	DEC	Digital-7-53-M
Maindec 701 (Instruction Test)*	DEC	Digital-7-54-M
Maindec 703 (Checkerboard)*	DEC	Digital-7-55-M
Maindec 702 (Address Test)*	DEC	Digital-7-56-M
Maindec 710 (RPB Test)*	DEC	Digital-7-57-M

* One is supplied with the equipment

5.3 MODULE HANDLING

Turn off all power before extracting or inserting modules. Access to controls on the module for use in adjustment, or access to points used in signal tracing can be gained by removing the module (use a straight, even pull to prevent twisting of the printed-wiring board), connecting a Type W980 FLIP CHIP Module Extender into the vacated module connector in the mounting panel, and then reinserting the module into the extender.

5.4 MAINTENANCE CONTROLS AND INDICATORS

In addition to the controls and indicators on the operator console, the indicator panel, and on the Teletype unit (described in chapter 2); maintenance operations use controls and indicators on the marginal-check panel (mounted at the top of bay 3, at the front of the computer) and on the Type 832 Power Control. Table 5-2 describes the function of these controls and indicators, and figure 5-1 shows the marginal-check panel.

TABLE 5-2 MAINTENANCE CONTROLS AND INDICATORS

Control or Indicator	Function
	Marginal-Check Panel
Voltmeter	Indicates the output voltage of the marginal-check power supply in either polarity.
Toggle switches (four)	The bottom switch applies a -10 marginal-check voltage to the Teletype control in the up position. The second switch from the bottom applies -15 marginal-check voltage to the Teletype control in the up position. The other two switches are not used.
Selector switch	Controls the output of the marginal-check power supply. In the +10MC position, the output is positive and is connected to the orange +10MC connector. In the -15MC position, the output is negative and is connected to the green -15MC connector. The center position is off and disconnects the output from the marginal-check power supply.

TABLE 5-2 MAINTENANCE CONTROLS AND INDICATORS (Cont)

Control or Indicator	Function
Elapsed time meter	Indicates the total number of computer operating hours. This unit of measure is instrumental for determining preventive maintenance schedules by recording time between similar malfunctions, etc.
Control knob	Controls the ourput of the marginal-check voltage to any level between 0 and 20v.
	Type 832 Power Control
Circuit breaker	Protects the computer circuits from overload due to failure of the computer power circuits.
REMOTE/OFF/LOCAL switch	Allows control of the computer primary power from the rear of the machine during maintenance. In the REMOTE position, the lock and POWER switches on the operator console control application and removal of computer power. In the OFF position the computer is de-energized, regardless of the position of switches on the operator console. In the LOCAL position the computer is energized regardless of the position of operator console switches or door interlocks.
MEM. POWER switch	Controls the application and removal of operating voltages for the memory circuits.

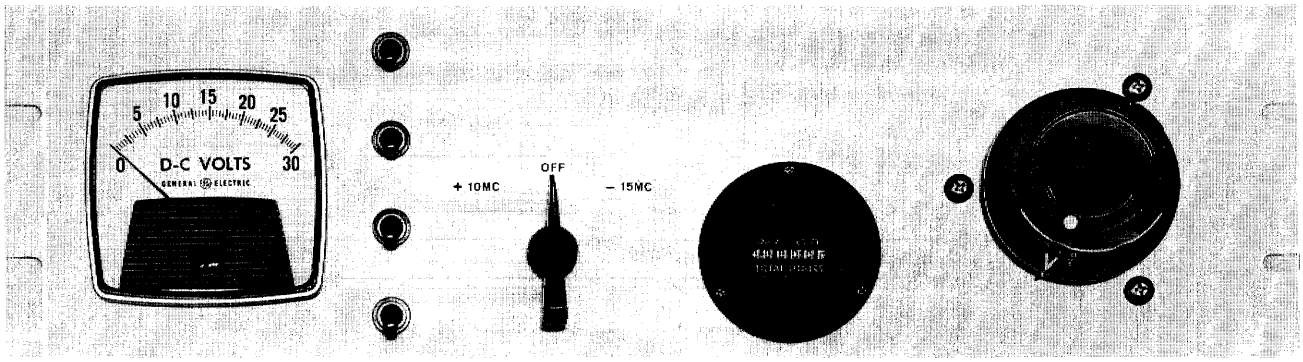


Figure 5-1 Marginal-Check Panel

5.5 PREVENTIVE MAINTENANCE

Preventive maintenance consists of tasks performed periodically during operating time of the equipment to ensure satisfactory working condition. Performance of these tasks forestalls failures caused by progressive deterioration or minor damage, which if not corrected causes eventual down-time. Data obtained during the performance of each task should be recorded in a log book. Analysis of this data indicates the rate of circuit operation deterioration and provides information for determining when components should be replaced to prevent failure of the system.

Preventive maintenance tasks consist of mechanical checks, i.e., cleaning and visual inspections; marginal checks, which aggravate border-line circuit conditions or intermittent failures for detection and/or correction; and checks of specific circuit elements such as the power supply, sense amplifiers and master slice control, and memory selectors. All preventive maintenance tasks should be performed on a schedule established by conditions at the installation site. The most important schedule to maintain is that of the mechanical checks, which should be performed monthly or as often as required to allow efficient functioning of the air filter, thus avoiding machine failures caused by overheating due to dirty air filters. All other tasks should be performed on a regular schedule, at an interval determined by the reliability requirements of the system. A typical recommended schedule is every 600 equipment operating hours or every four months, whichever comes first.

5.5.1 Mechanical Checks

a. Clean the exterior and the interior of the equipment cabinet using a vacuum cleaner or clean cloths moistened in nonflammable solvent.

b. Clean the air filters of the bottom of the cabinets. Remove each filter by removing the fan and housing, held in place by two knurled and slotted captive screws, and wash in soapy water and dry in an oven or by spraying with compressed gas. Spray each filter with Filter-Kote (Research Products Corporation, Madison, Wisconsin).

c. Lubricate door hinges and casters with a light machine oil, wiping off excess oil.

d. Repaint any scratched or corroded areas with DEC blue tweed paint number 5150-S65.

e. Inspect all wiring and cables for cuts, breaks, fraying, wear, deterioration, kinks, strain, and mechanical security. Tape, solder, or replace any defective wiring or cable covering.

f. Inspect the following for mechanical security: keys, switches, control knobs, lamp assemblies, jacks, connectors, transformers, fans, capacitors, elapsed time meter, etc. Tighten or replace as required.

g. Inspect all module mounting panels to assure that each module is securely seated in its connector.

h. Inspect power supply capacitors for leaks, bulges, or discoloration. Replace any capacitors giving these signs of malfunction.

5.5.2 Power Supply Checks

Perform the power supply output checks described in table 5-3. Use a multimeter to make the output voltage measurements with the normal load connected, and the oscilloscope to measure the peak-to-peak ripple content on all dc outputs of the supply. The +10 and -15v supplies are not adjustable therefore, if any output voltage or ripple content is not within specifications, consider defective the power supply giving these indications and initiate troubleshooting procedures. Refer to the engineering drawing listed in the table.

TABLE 5-3 POWER SUPPLY OUTPUT CHECKS

Measurement Terminals at Power Supply Output	Nominal Output (vdc)	Acceptable Output Range (v)	Maximum Output Current (amp)	Maximum Peak-to-Peak Output Ripple (v)
		Type 728 Power Supply Drawing (RS-B-728)		
Red (+) to Yellow (-)	+10	+9.5 to 11.5	7.5	0.7
Yellow (+) to Blue (-)	-15	-14.5 to 16.5	8.5	0.4
		Type 778 Power Supply Drawing (RS-B-778)		
Red (+) to Blue (-)	-15	-14.5 to 16.5	8.5	0.6
		Type 779 Power Supply Drawing (RS-B-779)		
Orange (+) to Yellow (-)	+10	+9.6 to 11.0	7.5	1.0
Yellow (+) to Blue (-)	-15	-14.5 to 16.0	8.0	0.4
Red (+) to Yellow (-)	+15	+14.5 to 16.0	7.5	1.1
Yellow (+) to Green (-)	+15	+14.5 to 16.0	7.5	1.1

Check the operation of the varible-output Type 738 Power Supply which produces the marginal-check voltages. With all of the normal/marginal switches in the normal (down) position, make the following measurements at the color-coded connector at the right side of any convenient module mounting panel:

a. Connect a multimeter between the yellow (-) and black (+) terminals; set the +10MC/OFF/-15MC switch to the -15MC position, and turn the control knob clockwise to assure that the supply can produce at least -20v (as indicated on the multimeter). Record the indication given on both the marginal-check voltmeter on the panel and on the multimeter. These indications should be equal, ±1v. Connect the oscilloscope to the yellow terminal, and measure the peak-to-peak repple content to assure that it is no more than 1.0v. Turn the control knob fully counterclockwise; set the +10MC/OFF/-15MC switch to the OFF position, and disconnect the multimeter and oscilloscope.

b. Connect the multimeter between the green (+) and black (-) terminals; set the +10MC/OFF/-15MC switch to the +10MC position, and turn the control knob clockwise to assure that the supply can produce at least +20v. Turn the control knob fully counterclockwise, set the +10MC/OFF/-15MC switch to the OFF position, and disconnect the multimeter.

The Type 739 Power Supply output is not measured during this check, since it is monitored and adjusted during the memory current check.

5.5.3 Marginal Checks

Marginal checking utilizes the Maindec diagnostic programs to test the functional capabilities of the computer with the module-operating voltages biased above and below the nominal levels. Biasing the operating voltages aggravates borderline circuit conditions within the modules to produce failures detected by the program (see description of diagnostics, paragraph 5.6.1). Upon error detection the program usually provides a printout or visual indication which aids in locating the source of the fault, and halts. Therefore, replacement of modules with marginal components is possible during scheduled preventive maintenance.

The biased operating voltages at which circuits fail are recorded in the maintenance log. By plotting the bias voltages obtained during each scheduled preventive maintenance, progressive deterioration can be observed and expected failure dates can be predicted, thus providing a means of planned replacement. These checks can also be used as a troubleshooting aid to locate marginal or intermittent components, such as deteriorating transistors.

Raising the operating voltages above +10v increases the transistor cutoff bias that the previous driving transistor must overcome, therefore low-gain transistors fail. Lowering the bias voltage below +10v

reduces transistor base bias and noise rejection, thus providing a test to detect high-leakage transistors. Lowering this voltage also simulates high-temperature conditions (to check for thermal run away). Raising and lowering the -15v supply increases and decreases the primary collector supply voltage for all modules and so affects output signal voltage.

Since the marginal voltages attainable vary for different circuit changes and/or system configurations, determine the expected marginal-check voltages for a specific system from the initial factory test records and any subsequent test records in the maintenance log. A record of margins obtained at the factory for a specific system is provided and serves as a base for all preventive and corrective maintenance procedures.

Margins decrease with time and normal circuit operation deterioration, but this decrease does not affect reliable operation of the machine until there is little or no margin at all. The normal slow rate of margin decay can be used to predict the time at which the system should be examined to prevent sudden failure; margins do provide a measure of circuit performance and can be used to certify correct or defective operation.

CAUTION

Do not increase the -15v margin beyond -18v. Failure to observe this precaution may cause serious damage to the logic elements.

Marginal-check voltages are supplied to the various sections of the processor through connections made to the module connectors in each mounting panel. Each marginal-check voltage may be adjusted throughout the range of 0 to 20v by means of the control knob and voltmeter located on the marginal-check control panel. The selector switch on this panel selects either the +10 or the -15 marginal-check voltage. Power supply leads to the module connectors in the mounting panels are color-coded as follows:

Orange	+10v marginal-check supply
Red	+10v normal power supply
Black	Ground
Blue	-15v normal power supply
Green	-15v marginal-check supply

Marginal-check and normal supply voltages are distributed to each of two module rows in each mounting panel through four SPDT switches on the marginal-check panel of each assembly. There are two positions for each SPDT switch: normal (down) and marginal-check (up). Therefore the modules in one row may be marginally-checked, all other rows maintaining normal voltage. In each row the upper switch controls

the +10v supply and the lower controls the -15v supply (with mounting panel viewed from the connector side and switches on the left).

To perform the checks:

a. Assure that all normal/marginal-check switches on each module mounting panel are in the normal (down) position (normal +10v and -15v power supplies are being used).

b. Set the +10MC/OFF/-15MC selector switch on the marginal-check control panel to the +10MC position.

c. Adjust the output of the marginal-check power supply so that the marginal-check voltmeter indicates 10v.

d. Set the +10 normal/marginal switch for the first row to be checked to the marginal-check (up) position.

e. Start computer operation in a diagnostic program or routine which fully utilizes the circuits in the row to be tested. If no program is suggested by the normal system application, select an appropriate Maindec program from table 5-4. To completely test the PDP-7, all Maindec programs listed in table 5-4 should be performed at elevated and reduced voltages for each supply terminal (+10, -15) and for each row indicated in the table.

f. Decrease the marginal-check power supply output until normal system operation is interrupted, and record the marginal-check voltage. At this point marginal transistors can be located and replaced, if desired. Readjust the marginal-check power supply output to the nominal +10v level.

g. Restart computer operation. Increase the marginal-check supply output until normal computer operation is interrupted, at which point record the marginal-check voltage. Again it is possible to locate and replace transistors. Readjust the marginal-check power supply to the nominal +10v level.

h. Return the normal/marginal switch to the normal (down) position.

i. Repeat steps d through h for each of the other rows to be checked by biasing the +10v line.

j. Set the +10MC/OFF/-15MC selector switch on the marginal-check power supply to the -15MC position and adjust the output until the marginal-check voltmeter indicates 15v.

k. Set the -15 normal/marginal switch to the marginal-check (up) position for the first row to be checked; then repeat step e.

l. Repeat steps f and g, readjusting the marginal-check power supply to the nominal -15v level at the end of each step. Return the normal/marginal switches to the normal (down) position.

m. Repeat steps j through l for each other row to be tested by biasing the -15v line.

n. Set the +10MC/OFF/-15MC selector switch to the OFF position.

5.5.4 Memory Current Check

Measure the read/write and inhibit currents in the core memory. These currents should equal the values specified on the memory array label (approximately 330 ma and 290 ma, respectively). This label indicates the optimum memory setting determined at the factory. Allow the equipment to warm up for approximately 1 hr before making measurements. Whenever possible this check should be performed at an ambient temperature of 25° C. Compensate measured read/write and inhibit currents by subtracting 1 ma for every degree of ambient temperature above 25° C. (Add 1 ma for each degree below 25° C.) The memory current check and sense amplifier check procedures must not be performed when the equipment temperature is below 20° C.

Measure the read/write current using the oscilloscope and clip-on current probe at the read side of a fully selected drive line of the X and Y axis G202 Memory Selector Switch. The READ terminals are either L and P, or M and N of a G202 module (refer to the G202 module schematic). Synchronize the oscilloscope with the negative transition of the READ signal found at location 1B202H. Adjust the read/write current to 330 ma or to the value specified on the memory array label by rotation of R16 in the G808 read/write power supply control module.

In a similar manner, measure the inhibit current by connecting the clip-on current probe at a proper terminal of the inhibit connector located at 1B10. See drawing G201 for the appropriate inhibit terminal. Synchronize the oscilloscope on the negative transition of the INH(B) line found at location 1B10J. Adjust the inhibit current to 290 ma or to the value indicated on the memory array label. To obtain consistent measurements, position the current probe to indicate read current as a negative pulse, and write and inhibit currents as positive pulses as displayed on the oscilloscope. Make all current amplitude measurements just before the knee in the curve of the trailing edge of a pulse. Note that read/write currents are measured from base line to peak amplitude, not from peak to peak.

TABLE 5-4 MARGINAL TEST PROGRAMS

Mounting Panel Row Tested	Diagnostic (MAINDEC) Test					
	Clock Interrupt Test Digital-7-51-M	Memory Checkerboard Test 703 Digital-7-55-M	Address Test 702 Digital-7-56-M	Contest II Digital-7-52-M	Reader and Punch Test Digital-7-53-M	Teleprinter Test Digital-7-50-M
CP 1C		+10				
CP 1D		+10		+10, -15		
CP 1E		+10		+10, -15		
CP 1F				+10, -15		
CP 1H	* ** +10, -15			+10, -15	+10, -15	+10, -15
CP 1J				+10, -15		
CP 1K				+10, -15		
CP 1L				+10, -15		
CP 1M				+10, -15		
CP 1N	* ** +10, -15			+10, -15		
CP 1P	* ** +10, -15			+10, -15	+10, -15	+10, -15

* This check made with third (from the top) toggle switch on marginal-check panel in the ON (up) position.
**This check made with bottom toggle switch on marginal-check panel in the ON (up) position.

TABLE 5-4 MARGINAL TEST PROGRAMS (continued)

Mounting Panel Row Tested	Diagnostic (MAINDEC) Test					
	Clock Interrupt Test Digital-7-51-M	Memory Checkerboard Test 703 Digital-7-55-M	Address Test 702 Digital-7-56-M	Contest II Digital-7-52-M	Reader and Punch Test Digital-7-53-M	Teleprinter Test Digital-7-50-M
MEM 1A		+10	+10			
MEM 1B		+10	+10			
MEM 1H		+10	+10			
MEM 1J		+10	+10			
DS 2A	* ** +10, -15				+10, -15	+10, -15
DS 2B	* ** +10, -15				+10, -15	+10, -15
DS 2C	* ** +10, -15				+10, -15	+10, -15
Reader/Punch 3A	* ** +10, -15				+10, -15	
Reader/Punch 3B	* ** +10, -15				+10, -15	
Teletype Control	* ** +10, -15					* ** +10, -15
Teletype Control						+10, -15

* This check made with third (from the top) toggle switch on marginal-check panel in the ON (up) position.
** This check made with bottom toggle switch on marginal-check panel in the ON (up) position.

5.5.5 Sense Amplifier Check

The G001 Sense Amplifier (SA) modules are adjusted using marginal-checking techniques. Perform the marginal checks using the Memory Checkerboard Program, Maindec 702. See table 5-4 for marginal-power supply used, and set the SPDT switches accordingly. Check and adjust each SA circuit so that approximately equal positive and negative margins can be obtained, using the +10v marginal power supply.

Sense amplifiers are located at 1H and 1J, 1-19. The master slice control is located at 1H20.

5.6 CORRECTIVE MAINTENANCE

Should a malfunction occur, the condition should be analyzed and corrected as indicated in the following procedures. No test equipment nor special tools are required for corrective maintenance other than a broad bandwidth oscilloscope and a standard multimeter. However, a clip-on current probe such as the Tektronix Type P6016 with a Type 131 Current Probe Amplifier is very helpful in monitoring memory currents. The best corrective maintenance tool is a thorough understanding of the physical and electrical characteristics of the equipment. Persons responsible for maintenance who are thoroughly familiar with the system concept, the logic drawings, operation of specific module circuits, and the location of mechanical and electrical components can readily interpret diagnostic routine printouts for isolating malfunctions.

Diagnosis and remedial action for a fault condition usually proceed by the following steps:

a. Preliminary investigation: gather all information to determine the physical and electrical security of the computer.

b. System troubleshooting: define the error by locating the fault to within a module through use of diagnostic routines, control panel troubleshooting, signal tracing, or aggravation techniques.

c. Replace defective module or modules to get the system on-line.

d. Log entry to record pertinent data.

Circuit troubleshooting to locate defective parts within a module and repairs to replace or correct the cause of the circuit malfunction can proceed after the system is again operable. Reparied modules should be subjected to validation tests to assure that the fault has been corrected.

Before commencing troubleshooting procedures record all unusual functions of the machine prior to the fault and all observable symptoms. In addition, note the program in progress, condition of operator console indicators, etc. This information should be referenced to the maintenance log to determine whether this type of fault has occurred before or if there is any cyclic history of this fault, and to ascertain how the condition was previously corrected.

When the entire machine fails, perform a visual inspection to determine the physical and electrical security of all power sources, cables, connectors, etc. Assure that the power supplies are working properly and that there are no power short circuits by performing the Power Supply Checks as described under Preventive Maintenance. Check the condition of the air filter in the bottom of the cabinet. If this filter becomes clogged, the temperature within the cabinet might rise sufficiently to cause marginal semiconductors to become defective.

5.6.1 Maindec Diagnostic Programs

Maindec routines are diagnostic programs designed to exercise or test specific functions within the computer system, and are available as perforated paper program tapes in read-in mode format. A detailed description of the program contained on tape, procedures for using the program, and information on analyzing the program printout accompanies each tape. These programs isolate the problem to a major functional unit but not to the individual module level. However, examination of the printout, observation of panel light conditions, and knowledge of the contents of the logic diagrams allow maintenance personnel to establish the particular module at fault.

The following paragraphs briefly summarize the function of each basic maintenance routine for testing the I/O functions of the PDP-7 system. Other test routines are available for optional equipment (see complete PDP-7 Program Listing).

a. Teleprinter Input/Output Test - (Digital-7-50-M)

Tests the input and output functions of the teleprinter in four checks:

(1) Repeating single character output line.

(2) Repeating character sequence output line.

(3) Input of a line message, followed by output of same message.

(4) Input of a character, output of same character.

b. Clock Interrupt Test - (Digital-7-51-M)

Tests operation of clock, interrupt, reader, punch and teleprinter in the interrupt mode. Checks operation of flags and I/O skip instructions.

c. CONTEST II - (Digital-7-52-M)

Tests instructions, memory, clock, program interrupt, and reader, punch and teleprinter.

d. Reader and Punch Test - (Digital-7-53-M)

Exercises and tests reader and punch. Reads or punches alphanumeric format tape; time can be varied between read and punch commands.

The following Maindec programs test instructions, and the processor and memory operations.

a. MAINDEC 701 - Instruction Test - (Digital-7-54-M)

Instruction test consists of twelve programs that check all instructions (except IOTs) processor registers and controls (including PC), checks indirect addressing and automatic indexing. Refer to the covering document for location details, etc.

b. MAINDEC 703 - PDP-7 Checkerboard - (Digital-7-55-M)

Creates worst possible noise conditions in memory. Then checks accuracy word by word. Four starting addresses provide selection of different noise patterns.

c. MAINDEC 702 - Address Test - (Digital-7-56-M)

Tests Type 149A Memory Module for proper address selection; therefore, can aid in checking memory address system including MA and MB registers, memory selection switches and all associated controls.

d. MAINDEC 710 Read Binary Test (RPB) - (Digital-7-57-M)

Tests photo-electric reader during binary operation. Program detects picking up and dropping of information and feed holes.

The Maindec diagnostic programs are particularly useful under marginal-checking conditions. Each covering document contains full particulars for loading the program, interpreting results and operating the PDP-7 for diagnostic testing. Chapter 2 contains instructions for loading and starting Maindec programs.

5.6.2 System Troubleshooting

Begin troubleshooting by performing the operation in which the malfunction was initially observed, using the same program, and thoroughly check the program for proper control settings. Assure that the PDP-7, and not the peripheral equipment, is actually at fault before continuing with corrective maintenance procedures. Faults in equipment, check with transmits or receive information, or improper connection of the system frequently gives indications very similar to those caused by computer malfunction. Faulty ground connections between peripheral equipment and the computer are a common source of trouble. From that portion of the program being performed and the general condition of the indicators, the logical section of the machine at fault can usually be determined.

If the fault has been isolated to the computer but cannot be immediately localized to a specific logic function, it can usually be determined to be within either the core memory or the processor logic circuits. Proceed to the Memory Troubleshooting or Logic Troubleshooting procedures. When the

location of a fault has been narrowed to a logic element, continue troubleshooting to locate the defective module or component by means of signal tracing. If the fault is intermittent, a form of aggravation test should be employed to locate the source of the fault.

5.6.2.1 Memory Troubleshooting - If the entire memory system fails, use the multimeter to check the outputs of the 739 Power Supply. Measure the voltages at the terminal strip as indicated on engineering drawing RS-B-739. Do not attempt to adjust this supply. If the supply is defective, troubleshoot it and correct the cause of the trouble; then adjust the output voltage by performing the Memory Current Check.

This discussion references the X and Y axis selection drawings, BS-E-149-0-46 and BS-E-149-0-47 and the memory control drawing KA77A-0-IO. Looking at the X and Y axis drawings, note that a core address is selected by a combination of two G202 switch selectors: one on the left side of the array; the other on the bottom of the array. READ or WRITE transitions, buffered by the BD module at location 1B30, trigger all G202 selectors which generate and distribute the actual read/write current or specific cores. In each axis, selection of the two G202 switches is accomplished by the bit configuration in the MA register. The actual read/write current pulses flow from the positive supply line, through a left G202 selector, through a horizontal core matrix line, through the core and diodes, down a vertical core matrix line to a bottom G202 selector, and into the negative return line.

A train of current spikes will be seen, and missing spikes will then represent malfunctioning addresses. Read currents are at terminals E and M; writer currents are at terminals K and P of each drive selector. Before loading a Maindec Address program to find specific address malfunction, trace the read/write gating pulses from the BD module at 1B30 and all the H and J terminals of every G202 module. A G202 Switch Selector module cannot select without the gating pulse. If the read/write currents are not as specified on the memory array labels, adjust the Type G800 control module current accordingly.

Perform the Memory Address Test program (Maindec 702) to locate defective core memory addresses. Complete the entire program and record all addresses which fail. Inspect the record of failure addresses for common bits. Refer to engineering drawings BS-E-149-0-46 and BS-E-149-0-47, and check the memory selectors that decode common bits of the failing addresses. Also check the associated resistor board and memory matrix module.

If an address is dropping bits, use the operator console to deposit all binary 1s in that address. Then examine that contents of the address to determine which bit position is not being set (contains a 0). Check the sense amplifier, inhibit driver, and resistor board for the associated bit. Also check the memory inhibit current as described in the Memory Current Check.

If an address is picking up bits, use the operator console to deposit all binary 0s in that address, and proceed as described in the previous paragraph.

To locate the cause of a specific address failure, use the oscilloscope and current probe to trace read and write current while performing a repetitive program such as the Memory Address Test program or the Memory Checkerboard Test program.

Perform the Memory Checkerboard Test program (Maindec 703) to troubleshoot all other memory conditions.

5.6.2.2 Logic Troubleshooting - If the instructions do not seem to be functioning properly, perform the Instruction Test program (Maindec 701). This test halts to indicate instructions that fail. When an instruction fails, as indicated by the operator console indicators when the program stops, or by the diagnostic printout that follows the error halt, consult the descriptive manual for the Maindec 701 to obtain an interpretation that will localize the fault.

If the computer interrupt system or the Teletype teleprinter do not seem to be functioning properly, perform the Teleprinter Test Program, Digital-7-50-M. If the tape reader or punch operation is questionable, perform the Reader and Punch Test (Digital-7-53-M) or the RPB Test (Maindec 710).

Refer to the Teletype and Digitronics documents (see table 1-2) for detailed maintenance information on the Model 33 KSR set, BRPE Tape Punch Set, and Model 2500 Perforated Tape Reader.

5.6.2.3 Signal Tracing - If the fault has been located within a functional logic element, program the computer to repeat an operation which uses all functions of that element. Use the oscilloscope to trace signal flow through the suspected logic element. Oscilloscope sweep can be synchronized by control signals or clock pulses, which are available on individual module terminals at the wiring side (front) of the equipment. Circuits transferring signals with external equipment are most likely to encounter difficulty. Trace output signals from the interface connector back to the origin, and trace input signals from the connector to the final destination. The signal tracing method can be used to certify signal qualities such as pulse amplitude, duration, rise time, and the correct timing sequence. Refer to the table on engineering drawing KA-77A-0-5 to check or adjust the timing of circuits in the main timing chain or special timing chain generators. If an intermittent malfunction occurs, signal tracing must be combined with an appropriate form of aggravation test.

5.6.2.4 Aggravation Tests - Intermittent faults should be traced through aggravation techniques. Intermittent logic malfunctions are located by the performance of marginal-check procedures as described under Preventive Maintenance.

Intermittent failures caused by poor wiring connections can often be revealed by vibrating modules while running a repetitive test program. Often, tapping a wooden rod held against the handles of a suspect panel of modules is a useful technique. By repeatedly starting the test program and vibrating

fewer and fewer modules, the malfunction can be localized to within one or two modules. After isolating the malfunction in this manner, check the seating of the modules in the connector; check the module connector for wear or misalignment, and check the module wiring for cold solder joints or wiring kinks.

5.6.3 Circuit Troubleshooting

Basic functions and specifications for standard system modules used in the PDP-7 are presented in the FLIP CHIP Module Catalog, C-105. Circuit schematics are provided in chapter 6 for modules not described in the catalog. Schematic diagrams of all modules are provided in the set of formal engineering drawings supplied with each system. The following design considerations may also be helpful in troubleshooting standard modules.

a. Forward-biased silicon diodes are used in the same manner as Zener diodes, usually to provide a voltage differential of 0.75v. For instance, a series string of four diodes produces the −3 vdc clamp voltage used in most modules.

b. An incoming pulse which turns off the conducting transistor amplifier changes the state of DEC flip-flops. Since these flip-flops use PNP transistors, the input pulse must be positive and must be coupled to the base of the transistor. Flip-flop modules that accept negative pulses to change the state invert this pulse by means of a normal transistor inverter circuit.

c. Fixed-length delay lines such as the W300 are extremely reliable and ver seldom malfunction. However malfunction occurs, these delay lines should not be replaced on the printed-wiring board. In such cases return the entire module to DEC for repair.

d. The W607 and W640 modules both contain three independent pulse amplifiers, each with its own input inverter. The time required to saturate the interstate coupling transformer determines output pulse duration. No multivibrators or other RC timing circuits are used in the pulse amplifiers.

5.6.3.1 In-Line Dynamic Tests - To troubleshoot a module while maintaining its connection within the system:

a. De-energize the computer.

b. Remove the suspect module from the mounting panel.

c. Insert a W980 FLIP CHIP Module Extender into the mounting panel connector holding the suspect module.

d. Insert the suspect module into the module extender, making accessible all components and wiring points of the module.

e. Energize the computer and establish the program conditions desired for troubleshooting the module. Trace voltages or signals through the module, using a dc voltmeter or an oscilloscope, locating the source of the fault.

5.6.3.2 In-Line Marginal Checks - The normal marginal-checking method can perform checks of individual modules within the computer to test specific modules of questionable reliability, or to further localize the cause of an intermittent failure which has been localized to within one module row. These checks are performed with the aid of a modified W980 FLIP CHIP Module Extender. To modify an extender for these checks:

a. Disconnect module receptacle terminals A, B, and C from the male plug connection terminals. This can be accomplished by cutting the printed wiring for these lines near the plug end and removing a segment of this wiring in each line.

b. Solder a 3-ft test lead to the printed wiring for terminals A, B, and C. Make this solder joint close to the receptacle end of the extender, certainly on the receptacle side of the wiring break. Observe the normal precautions when making this connection to assure that excessive heat does not delaminate the printed-wiring board and that neither solder nor flux provides conduction between lines.

c. Attach a spade lug, such as an AMP 42025-1 Power Connector, to the end of each test lead and label each lead to correspond to the A, B, or C terminal of the receptacle to which it is connected.

To marginal check a module within the computer:

a. De-energize the computer.

b. Remove the module to be checked from the module mounting panel; replace it with the modified extender, and insert the module in the extender.

c(1). If the +10v marginal check is to be performed, connect test lead A to the +10v orange connector terminal at end of the panel. Connect test lead B to the normal −15v blue connector terminal and test lead C to black ground connector.

c(2). When performing the −15v marginal check, connect test lead A to the normal +10v red connector, test lead B to the −15v green connector terminal, and test lead C to the black ground terminal, keeping all SPDT switches in the down position.

d. Restore computer power, adjust the marginal-check power supply to provide the nominal voltage output, and start operation of a routine which fully utilizes the module being checked. The procedures and routines suggested in Preventive Maintenance for use in marginal checking the computer can be used as a guide to marginal-checking modules.

e. Increase or decrease the output of the marginal-check power supply until the routine stops, indicating module failure, and record each bias voltage at which the module fails. Also record the condition of all operator console controls and indicators when a failure occurs. This information indicates the module input conditions at the time of the failure and aids in tracing the cause of the fault to a particular component part.

f. Repeat steps d and e for each of the three bias voltages. If margins of ±5v on the +10 vdc supplies can be obtained, and the −15 vdc supply can be adjusted between −7v and −18v without module failure, it is assumed a module is operating satisfactorily. If the module fails before these margins are obtained, use normal signal tracing techniques within the module to locate the source of the fault.

5.6.3.3 Static Bench Tests - Visually inspect the module on both the component and printed-wiring sides to check for short circuits in the etched wiring and for damaged components. If this inspection fails to reveal the cause of trouble or to confirm a fault condition observed, use the multimeter to measure resistances.

CAUTION

Do not use the lowest or highest resistance ranges of the multimeter when checking semiconductor devices. The X10 range is suggested. Failure to heed this warning may result in damage to components.

Measure the emitter-collector, collector-base, and emitter-base resistances of transistors in both directions. A good transistor indicates an open circuit in both directions between collector and emitter. Normally 50 to 100 ohms exist between the emitter and the base or between the collector and the base in the forward direction, and open-circuit conditions exist in the reverse direction. To determine forward and reverse directions, consider a transistor as two diodes connected back-to-back. In this analogy PNP transistors are considered to have both cathodes connected together to form the base, and both the emitter and collector assume the function of an anode. In NPN transistors the base is assumed to be a common-anode connections, and both the emitter and collector are assumed to be the cathode.

Multimeter polarity must be checked before measuring resistances, since many meters (including the Triplett 630) apply a positive voltage to the common lead when in the resistance mode. Note that although incorrect resistance readings are a sure indication that a transistor is defective, correct readings give no guarantee that the transistor is functioning properly. A more reliable indication of diode or transistor malfunction is obtained by using one of the many inexpensive in-circuit testers commercially available.

Damage or cold-solder connections can also be located using the multimeter. Set the multimeter to the lowest resistance range and connect it across the suspected connection. Poke at the wires or components around the connection, or alternately rap the module lightly on a wooden surface, and observe the multimeter for open-circuit indications. Often the response time of the multimeter is too slow to detect the rapid transients produced by intermittent connections. Current interruptions of very short duration, caused by an intermittent connection, can be detected by connecting a 1.5v flashlight battery in series with a 1500-ohm resistor across the suspected connection. Observe the voltage across the 1500-ohm resistor with an oscilloscope, while probing the connection.

5.6.3.4 Dynamic Bench Tests - In general, return to DEC for repair or replacement a module which fails marginal in-line tests, or considered faulty for other reasons. Many modules require special equipment for dynamic testing, since the timing of pulse amplifiers and delay modules must be rigorously maintained within narrow limits. Dynamic tests, therefore, should be oriented only toward discovery of defective semiconductors. Dynamic tests may be carried out by means of a Type H901 Patchcord Mounting Panel connected to the computer power supply outputs by means of Type 914 Power Jumpers. Simulated ground-level signals may then be applied to the module under test, using Type 911 Patchcords, and an oscilloscope connected to terminals on the front of the Type H901 panel can monitor output terminals of the module under test.

5.6.4 Module Repair

Repairs to FLIP CHIP modules should be limited to the replacement of semiconductors. In all soldering and unsoldering operations in the repair and replacement of parts, avoid placing excessive solder or flux on adjacent parts or service lines. When soldering semiconductor devices (transistors, crystal diodes, and metallic rectifiers) which may be damaged by heat, the following special precautions should be taken:

1. Use a heat sink, such as a pair of pliers, to grip the lead between the device and the joint being soldered.

2. Use a 6v soldering iron with an isolation transformer. Use the smallest soldering iron adequate for the work.

3. Perform the soldering operation in the shortest possible time, to prevent damage to the component and delamination of the module etched wiring.

CHAPTER 6
ENGINEERING DRAWINGS

6.1 INTRODUCTION

This chapter contains reduced copies of DEC block schematics, circuit schematics, and other engineering drawings necessary for understanding and maintaining this equipment. Only those drawings which are essential and not available in the referenced pertinent documents are included. Should any discrepancy exist between the drawings in this chapter and those supplied with the equipment, assume the latter drawings to be correct. A complete listing of the drawings in this chapter is presented in the table of contents.

6.2 DRAWING NUMBERS

DEC engineering drawing numbers contain five groups of information, separated by hyphens. A drawing number such as BS-D-9999-1-5 consists of the following information reading from left to right: a 2- or 3-letter code specifying the type of drawing (BS); a 1-letter code specifying the original size of the drawing (D); the type number of the equipment (9999); the manufacturing series of the equipment (1); and the drawing number within a particular series (5). The drawing type codes are:

BS, block schematic or logic diagram
CL, cable list
FD, flow diagram
ML, module list
RS, replacement schematic
WD, wiring system

6.3 CIRCUIT SYMBOLS

The block schematics of DEC equipment are multipurpose drawings that combine signal flow, logical function, circuit type and physical location, wiring, and other pertinent information. Individual circuits are shown in block or semiblock form, using special symbols which define circuit operation. These symbols are similar to those appearing in both the FLIP CHIP Modules Catalog and the System Modules Catalog but are often simplified. Figure 6-1 illustrates some of the symbols used in DEC engineering drawings.

6.4 LOGIC SIGNAL SYMBOLS

DEC standard logic signal symbols are shown at the input of most circuits to specify the enabling conditions required to produce a desired output. These symbols represent either standard DEC logic levels, standard DEC pulses, standard FLIP CHIP pulses, or level transitions.

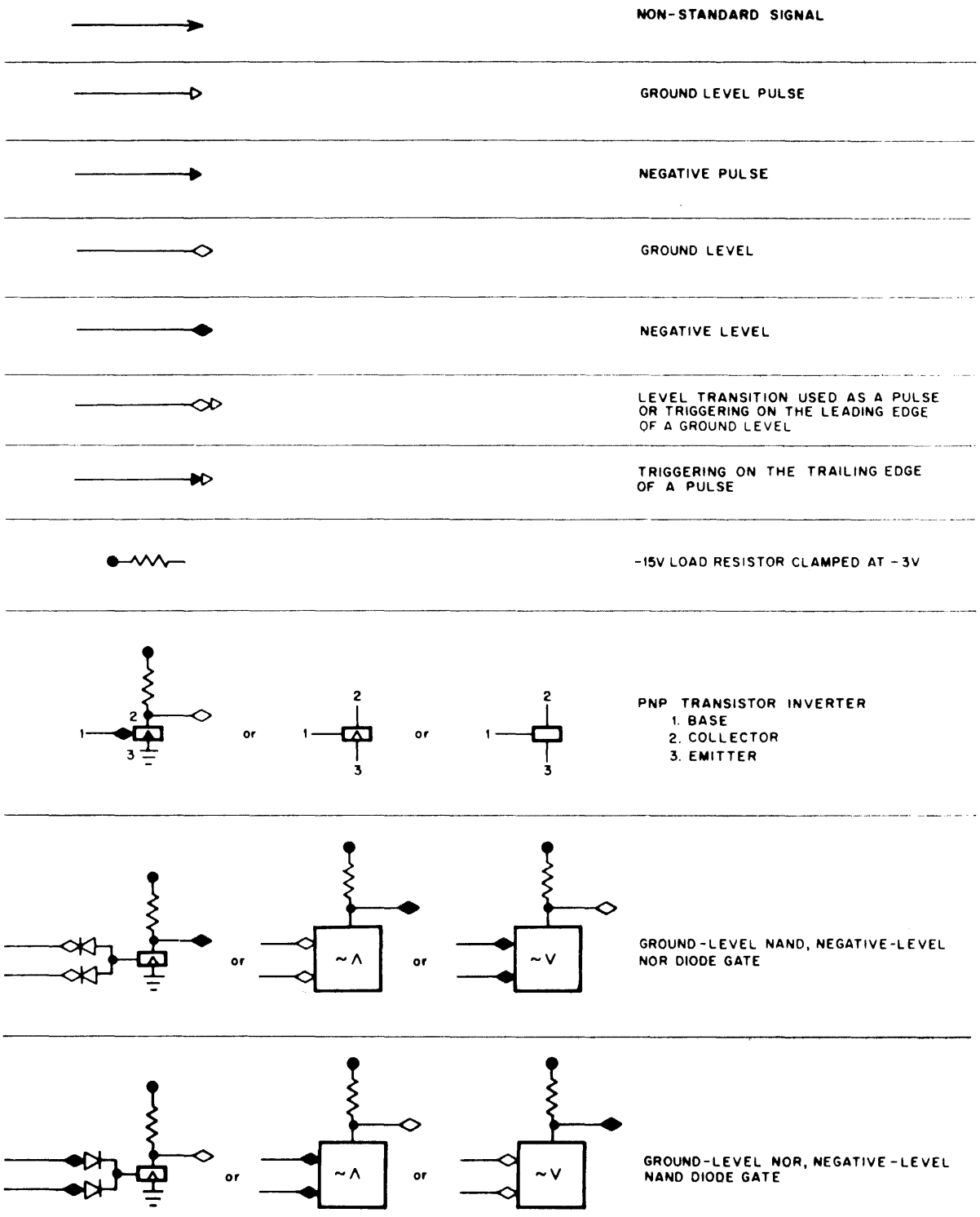
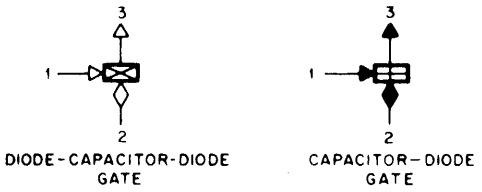
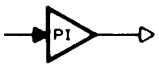


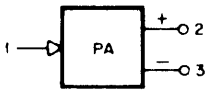
Figure 6-1 DEC Symbols



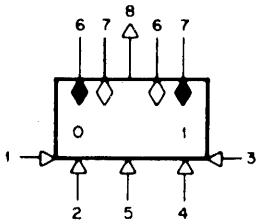
1. PULSE INPUT
2. CONDITIONING LEVEL INPUT
3. PULSE OUTPUT



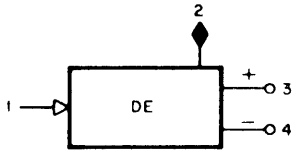
PULSE INVERTER



PULSE AMPLIFIER
1. PULSE INPUT, POLARITY INDICATED BY INPUT SIGNAL
2,3. TRANSFORMER-COUPLED PULSE OUTPUT. EITHER TERMINAL MAY BE GROUNDED



FLIP-FLOP (MOST FLIP-FLOPS HAVE ONLY SOME OF THE FOLLOWING):
1. DIRECT-CLEAR INPUT
2. GATED-CLEAR INPUT
3. DIRECT-SET INPUT
4. GATED-SET INPUT
5. COMPLEMENT INPUT
6. OUTPUT LEVEL, -3 V IF 0, 0 V IF 1
7. OUTPUT LEVEL, 0 V IF 0, -3 V IF 1
8. CARRY PULSE OUTPUT, UPON BEING CLEARED



DELAY (ONE-SHOT MULTIVIBRATOR)
1. INPUT PULSE
2. OUTPUT LEVEL, -3V DURING DELAY
3,4 TRANSFORMER-COUPLED PULSE OUTPUT. EITHER TERMINAL MAY BE GROUNDED

Figure 6-1 DEC Symbols (continued)

6.4.1 Logic Levels

The standard DEC logic level is either at ground (0 to −0.3v) or at −3v (−2.5 to −3.5v). Logic signals are given mnemonic names indicating the condition represented by assertion of the signal. An open diamond (——◇) indicates that the signal is a DEC logic level and that ground represents assertion; a solid diamond (——◆) indicates that the signal is also a DEC logic level and that −3v represents assertion. All logic signals applied to the conditioning level inputs of capacitor-diode gates or diode-capacitor-diode gates must be present for a specified length of time (depending on the module used) before an input pulse triggers operation of the gate.

6.4.2 Standard Pulses

DEC standard pulses are 2.5v in amplitude with reference to either ground or −3v, depending upon the type of module used. The width of standard pulses is either 40, 70, or 400 nsec as required for specific circuit configurations. The standard 2.5v negative pulse (−2.3 to −3.5v) is indicated by a solid triangle (⟶▶) and is always referenced with respect to ground, as shown in figure 6-2.

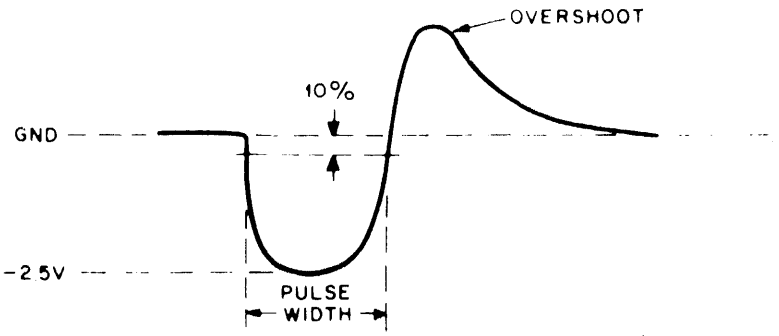


Figure 6-2 Standard Negative Pulse

The standard positive pulse is the inverse of the negative pulse and is indicated by an open triangle (⟶▷). The positive pulse goes either from −3v to ground or goes from ground to +2.5v (+2.3 to +3.0v).

6.4.3 FLIP CHIP Standard Pulses

Two types of pulses, R series and B series, are utilized in FLIP CHIP circuit operation. The pulse produced by R-series modules starts at −3v, goes to ground (−0.2v) for 100 nsec, then returns to −3v. This pulse appears in figure 6-3.

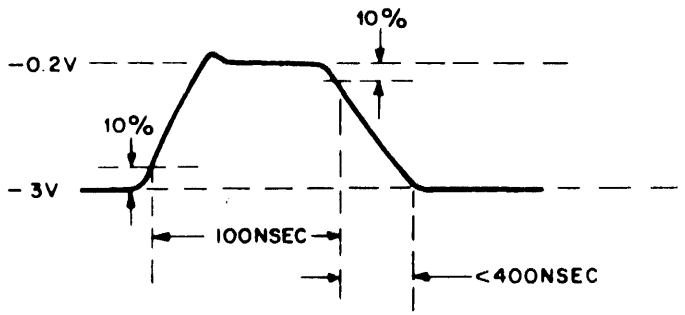


Figure 6-3 FLIP CHIP R-Series Pulse

The B-series negative pulse is 2.5v in amplitude and 40 nsec in duration and is similar to the one shown in figure 6-2. If this pulse is applied to the base of an inverter, the inverter output will be a narrow pulse, similar in shape to the R-series standard pulse. The B-series positive pulse, which goes from ground to +2.5v, is the inverse of the B-series negative pulse.

6.4.4 Level Transitions

Occasionally, the transition of a level is used at an input where a standard pulse is otherwise expected and a composite symbol (—◆▷) is drawn to indicate this fact. The triangle is drawn open or solid depending respectively on whether the positive (−3v to ground) or the negative (ground to −3v) transition triggers circuit action. The shading of the diamond either is the same as that of the triangle to indicate triggering on the leading edge of a level, or is opposite that of the triangle to indicate triggering on the trailing edge. An arrowhead (—▶) pointing in the direction of signal flow indicates nonstandard signals (power supply outputs, calibration reference levels, etc.).

6.5 COORDINATE SYSTEM

Each engineering logic drawing is divided into 32 zones (4 horizontal and 8 vertical) by marginal map coordinates. Figure references in the text are usually followed by a letter and a digit specifying the zone in which the referenced circuit is located. Physical reference to a drawing area such as "lower left" or "upper center" may also be used.

6.6 MODULE IDENTIFICATION

Two designations appear in or near each circuit symbol or inside the dotted line surrounding multiple circuit symbols shown on engineering drawings. The upper designation consists of four characters specifying the module type. This designation identifies modules in the Digital Systems Modules Catalog, and the FLIP CHIP Modules Catalog describes the FLIP CHIP modules. This manual or other referenced pertinent documents describes modules not found in either catalog.

The lower designation is the module location code. The leftmost character of this designation is a number indicating the cabinet in which the module is located. The next character is a letter indicating the mounting panel in which the module is located. The last character consists of one or two numbers specifying the module location within the mounting panel. As an example, the designation 1A22 indicates that this module is mounted in location 22 of mounting panel A in cabinet 1. Terminal J of this module is designated at 1A22J.

Module mounting panels which can accommodate more than one row of modules may be used in the construction of certain equipment. For this equipment, a letter is assigned to each row of modules within a mounting panel. When a particular device is contained within one cabinet, the number 1 may be omitted from the reference designations appearing on the associated drawings for that device.

Certain modules are indicated on engineering drawings by the normal 4-digit type number followed by the suffix R or by a number and R. These modules contain removable jumpers which connect certain output terminals to clamped load resistors. The suffix R indicates that all clamped load resistors on that particular module are in use; and since replacement modules are shipped with all calmped load

resistors connected, a new module can be substituted for the old without modifications. A suffix such as 2R indicates that the two clamped load resistors connected to output terminals designated by letters closest to the beginning of the alphabet are to remain connected, and all remaining jumpers connecting clamped load resistors to output terminals should be removed. As an example, the designation 1103-3R indicates that the jumpers associated with output terminals H, L, and P of a Type 1103 Inverter Module are to remain connected, while the jumpers associated with output terminals T, W, and Z, are to be removed, thereby modifying the standard Type 1103 into a Type 1103-3R.

6.7 EXAMPLE

Figure 6-4 illustrates DEC symbols and nomenclature. The circuit shown is a Type 4303 Integrating Single Shot used to control the enabling time of several gates. The module is located in the twelfth position from the left (when viewed from the front or wiring side) of mounting panel B (the second row of modules from the top) in cabinet 1. The symbol marked DELAY is a monostable multivibrator with two complementary outputs, terminals U and W. The output at terminal U is connected to terminals 2D18F and 1B15M while the output at terminal W is connected to terminal 1D02F.

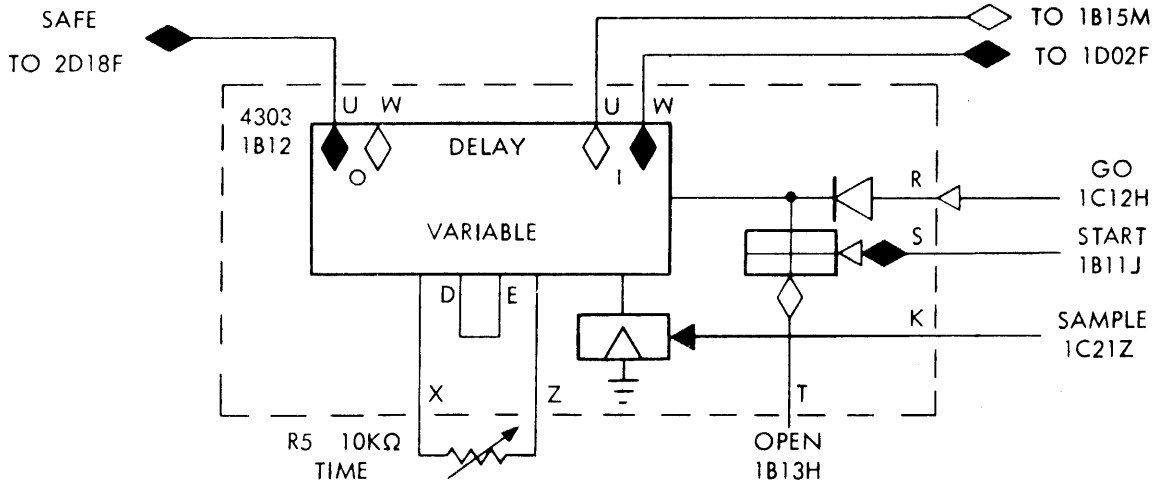
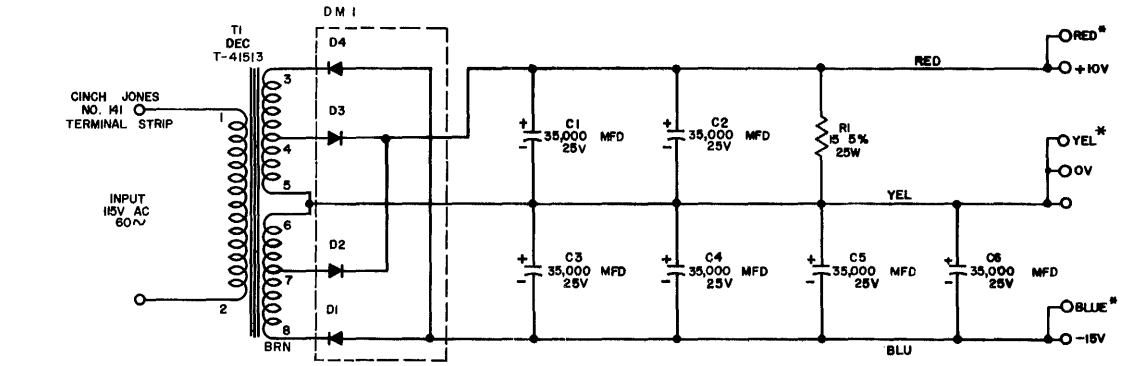


Figure 6-4 Typical DEC Logic Block Diagram

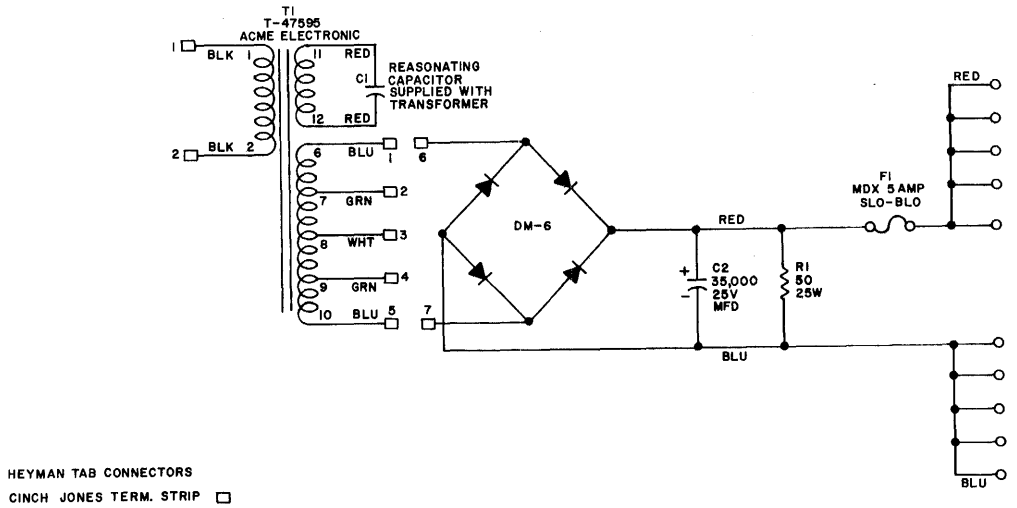


NOTE:
IN ORDER TO KEEP OUTPUT VOLTAGE WITHIN THE FOLLOWING LIMITS:
+10V: +9.5 TO +11V
-15V: -14.5 TO -16V
THE LOADING SHOULD BE WITHIN THE FOLLOWING LIMITS:

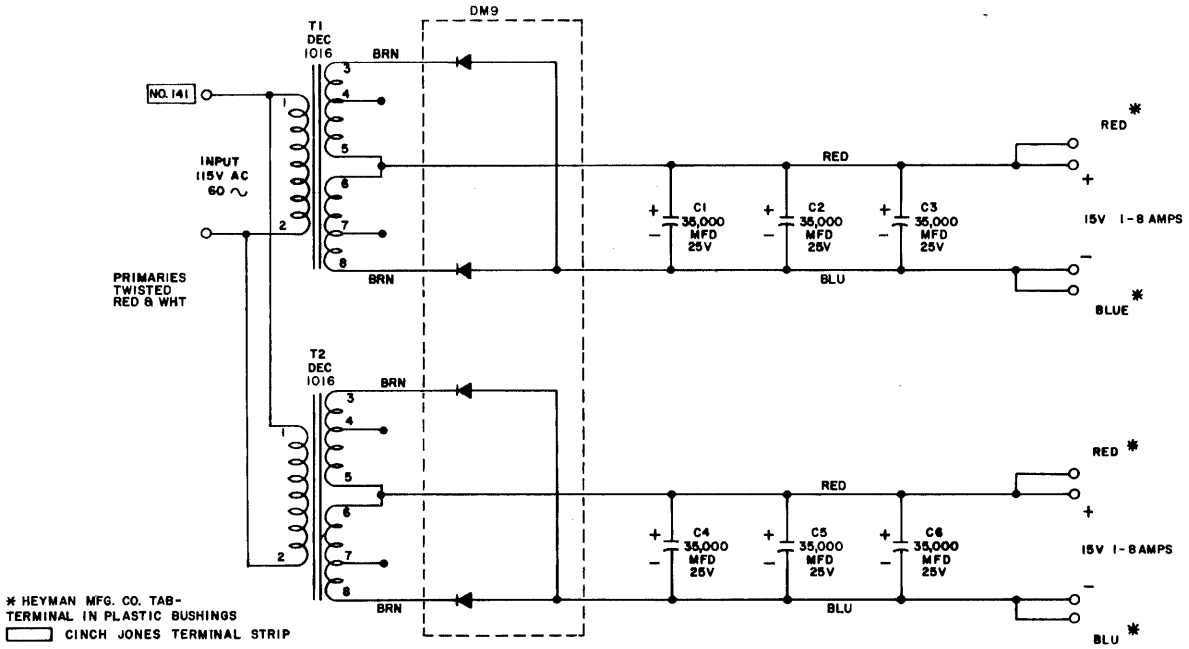
BOTH SIDES	+10 V	0	TO	7.0	AMPS
LOADED	-15 V	1.0	TO	8.0	AMPS
ONE SIDE	+10 V	0	TO	7.5	AMPS
LOADED	-15 V	1.0	TO	8.5	AMPS

SUM OF THE OUTPUT CURRENTS ARE LIMITED BY THE FOLLOWING EQUATION: $5I_{10} + 6I_{15} \leq 53$

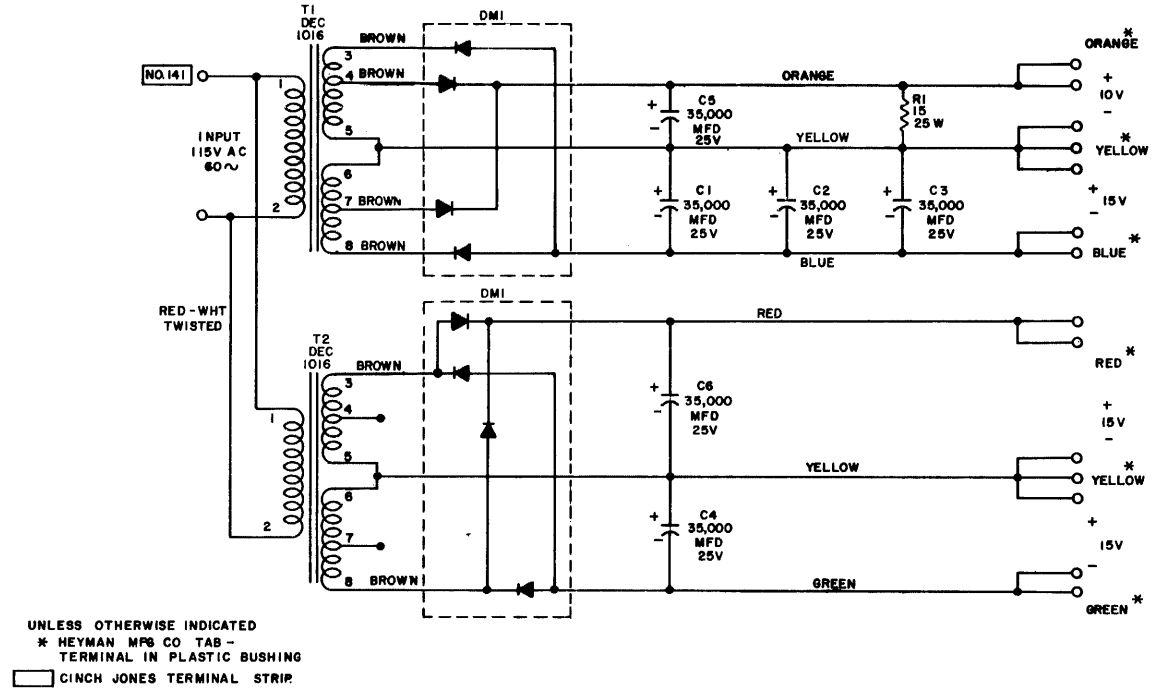
Power Supply (+10 and −15) RS-B-728



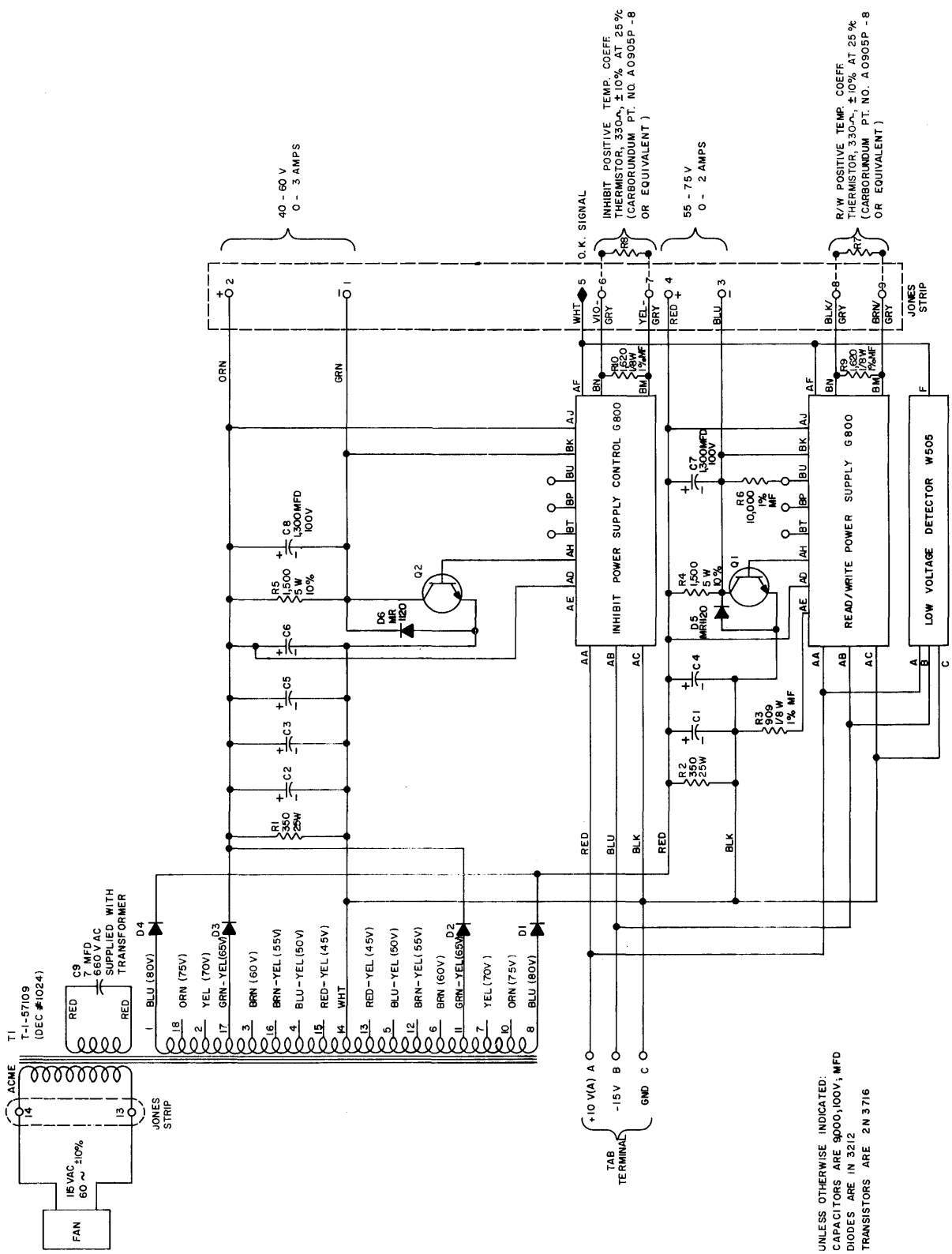
Power Supply (0-20 marginal check supply) RS-B-738



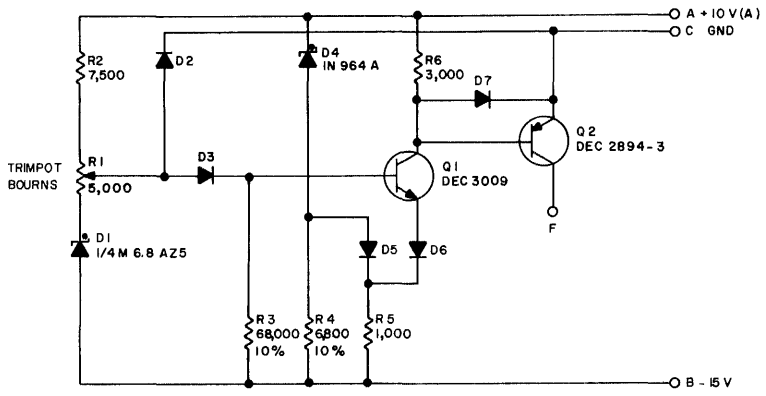
Dual 15-Volt Power Supply RS-B-778



Power Supply (one 10v and three 15v floating supplies) RS-B-779

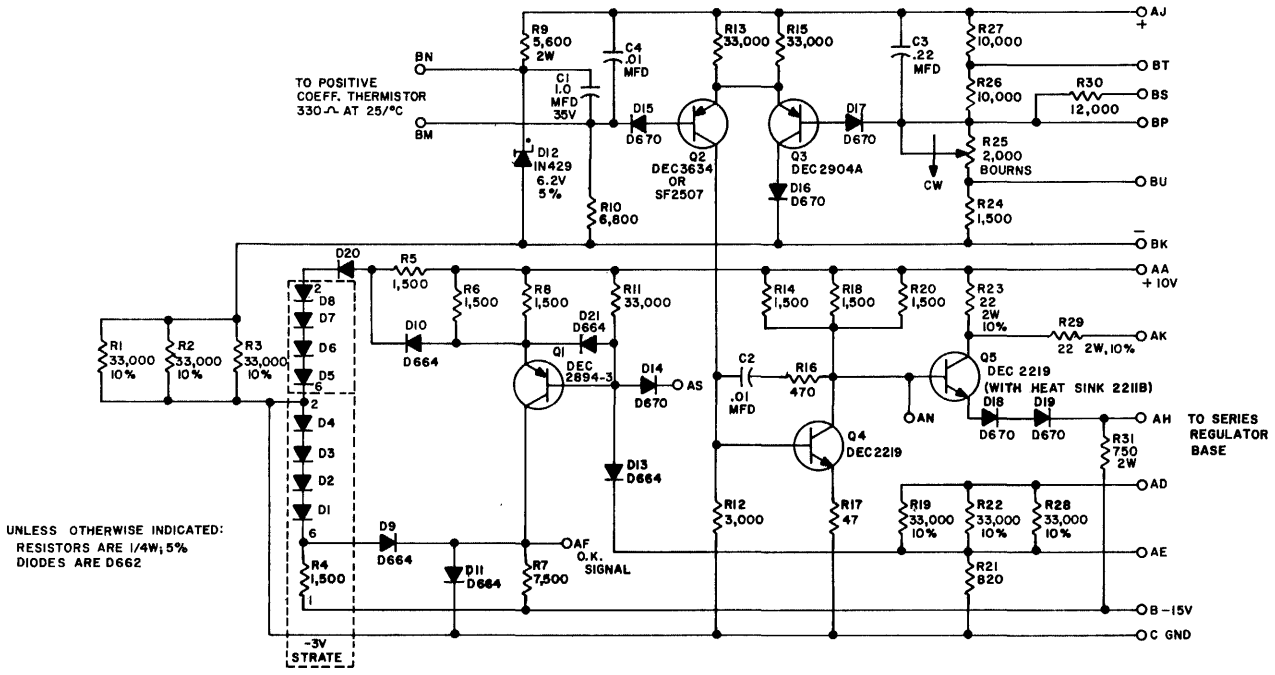


Power Supply (Memory) RS-C-739

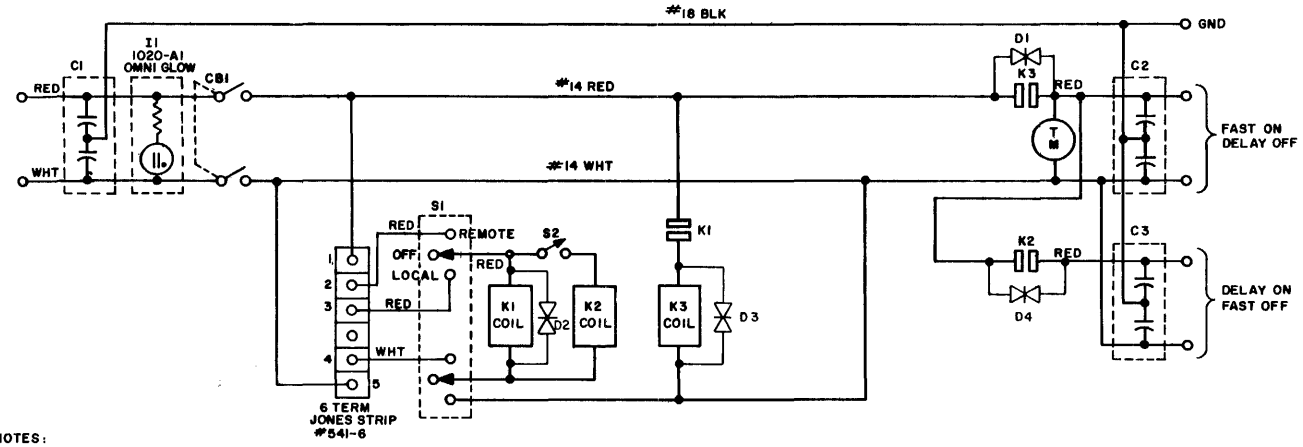


UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W, 5%
DIODES ARE D-664

Low-Voltage Detector (for 739) RS-B-W505



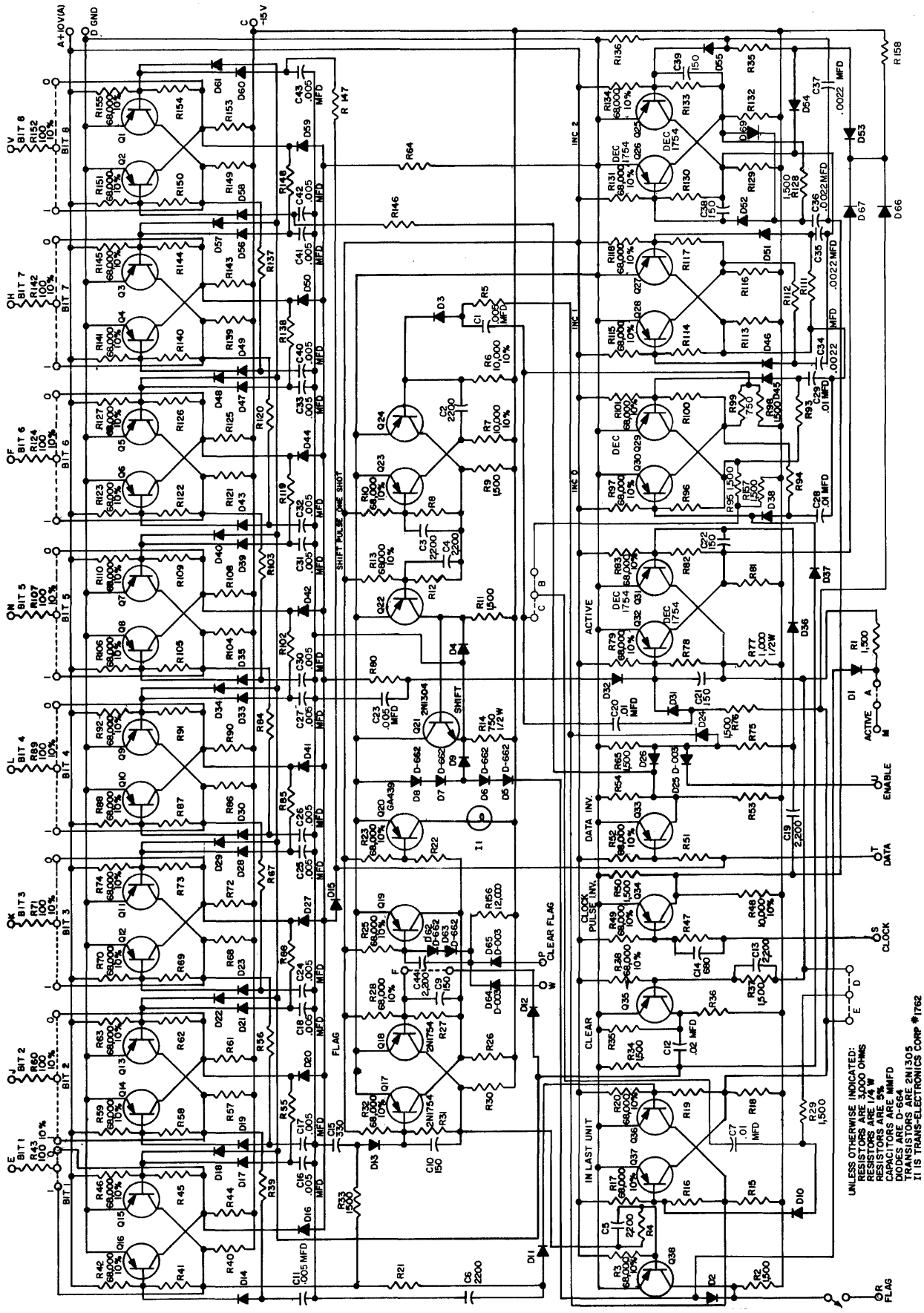
Control for 739 Power Supply RS-B-G800



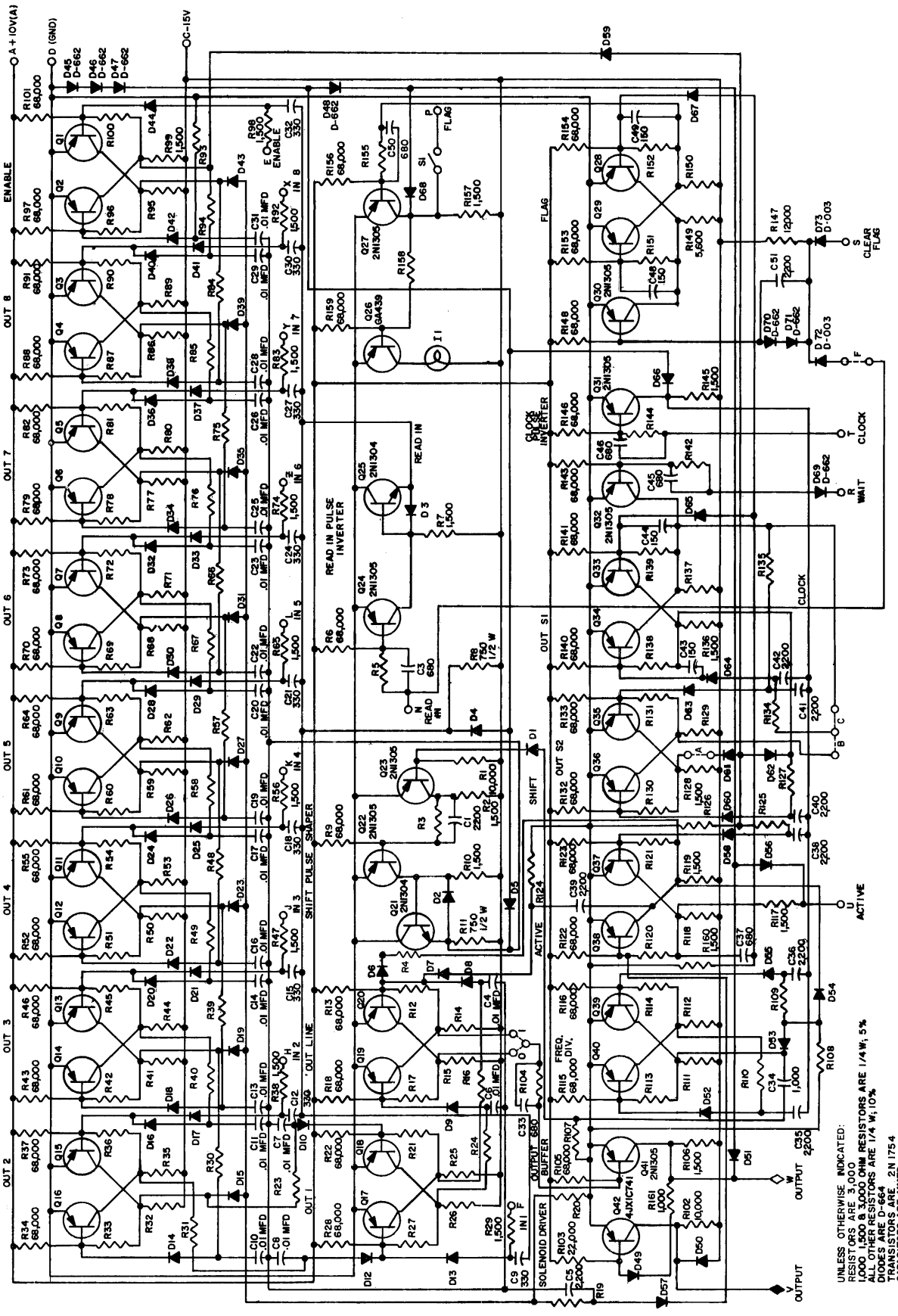
NOTES:

D1,D2,D3,D4 THYRECTOR GENERAL ELECTRIC 20SP 484,115V
C1 CAPACITOR 2 X.1 MFD 1000VDC #YAT 10011
CORNELL DUBLIER.
C2 & C3 CAPACITOR BATHTUB-DEC PURCH. SPEC #CAF-0001
2X.1MFD 600VDC CORNELL DUBLIER.
S1 TOGGLE SWITCH #ST52P.
S2 TOGGLE SWITCH SPDT 2 POS #7505-K3
K1 RELAY #1040-8-687 NORMALLY OPEN 115VAC COIL 3-5 SEC DELAY
QUICK OPERATE, SLOW RELEASE.
K2 RELAY #1040-8-58 NORMALLY OPEN 115 VAC COIL 3-5 SEC DELAY
SLOW OPERATE QUICK RELEASE.
K3 RELAY #EM-1 115VAC EBERT ELECTRONICS.
CB1 CIRCUIT BREAKER #190-220-101 20AMPS 250V, 60 CYC-CURVE 4

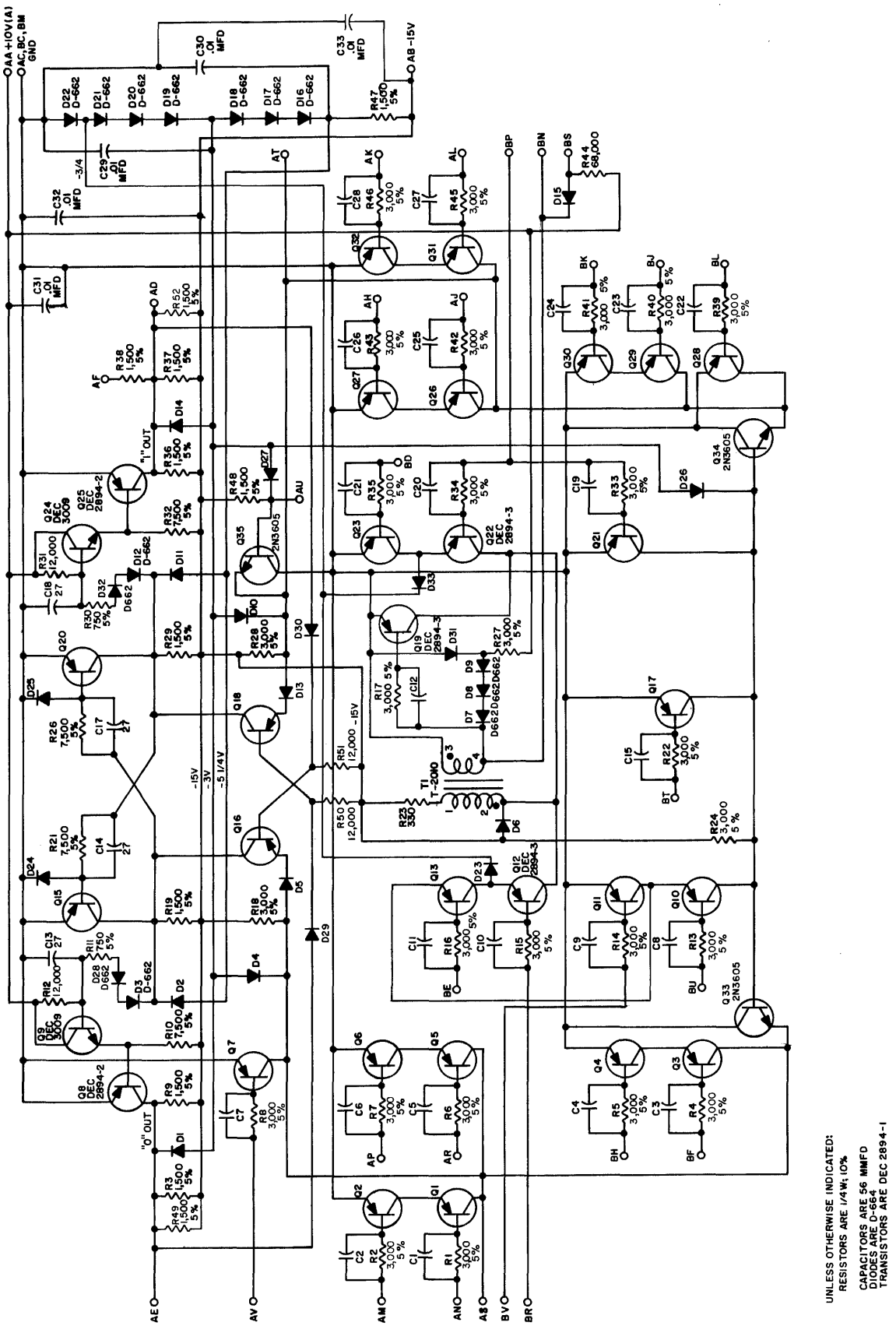
Two-Step Power Control RS-B-832



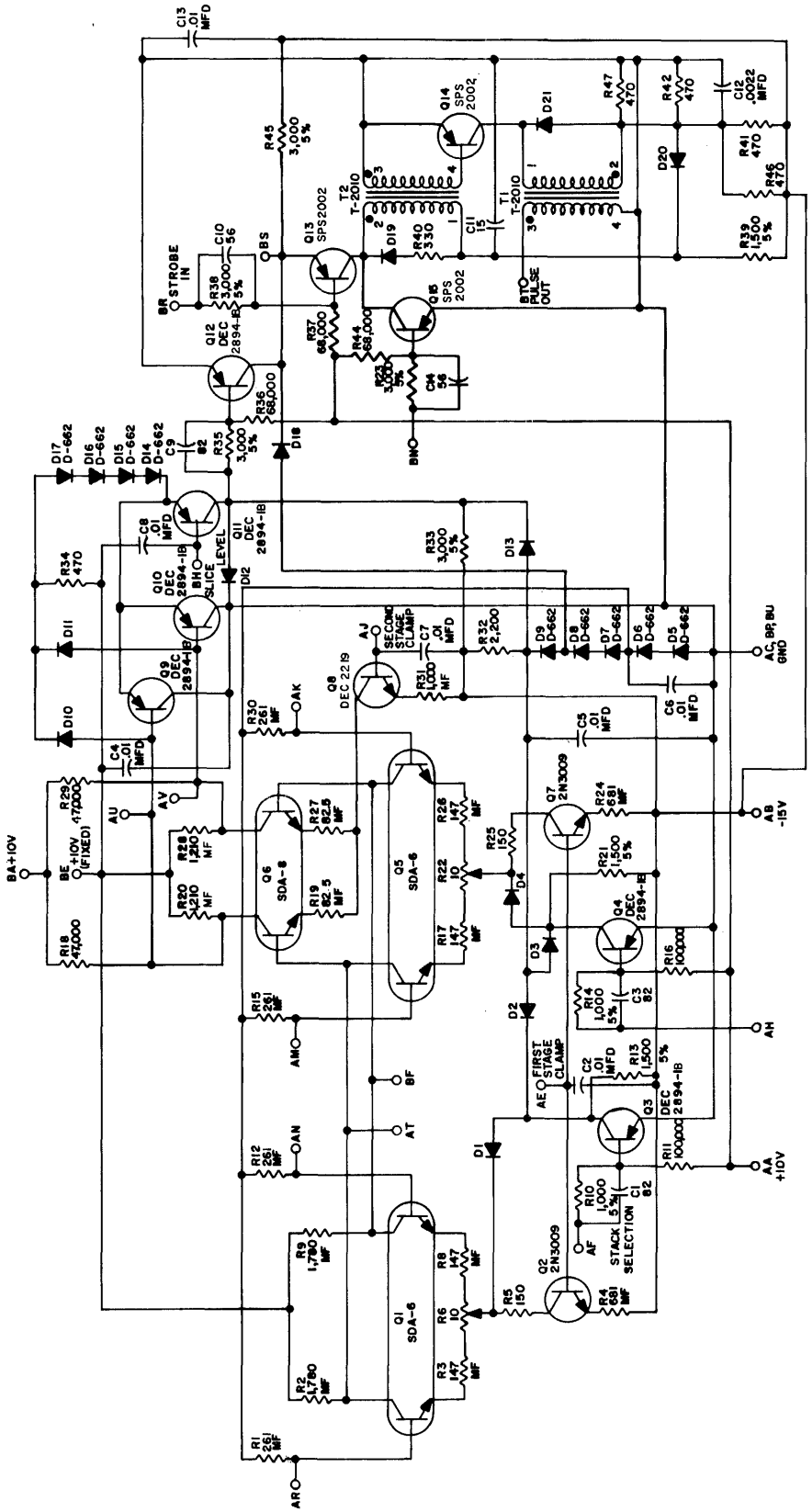
Eight-Bit Teletype Receiver RS-C-4706



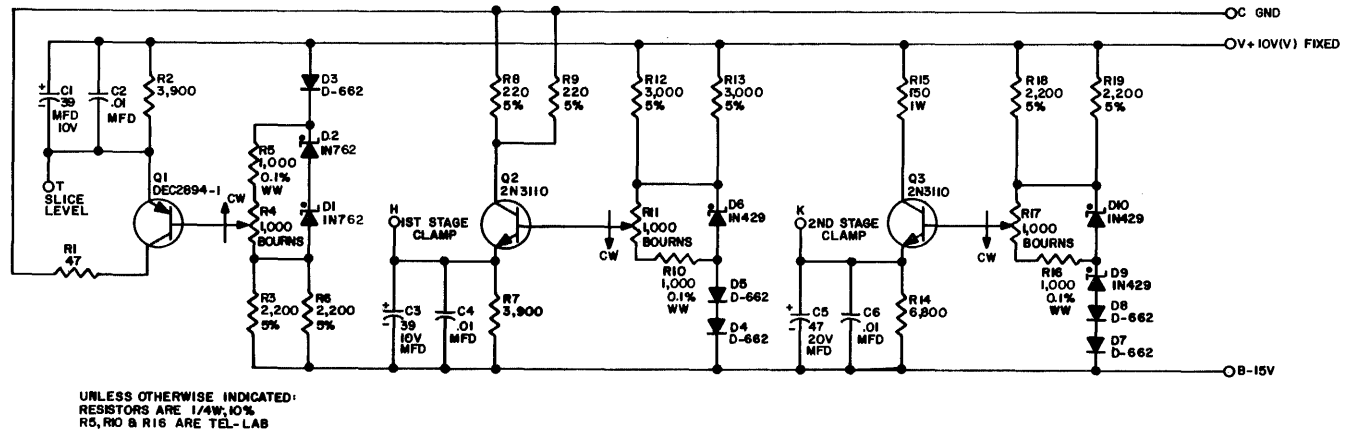
Eight-Bit Teletype Transmitter RS-C-4707



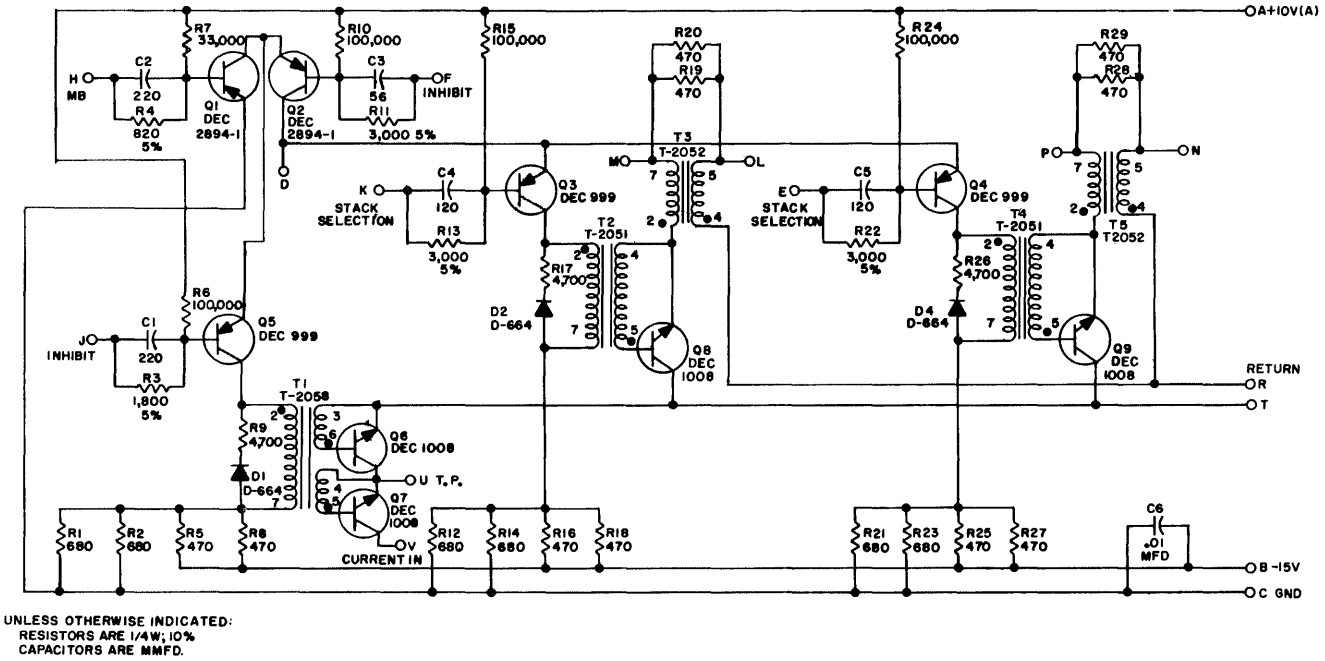
PDP-7 Accumulator RS-C-B210



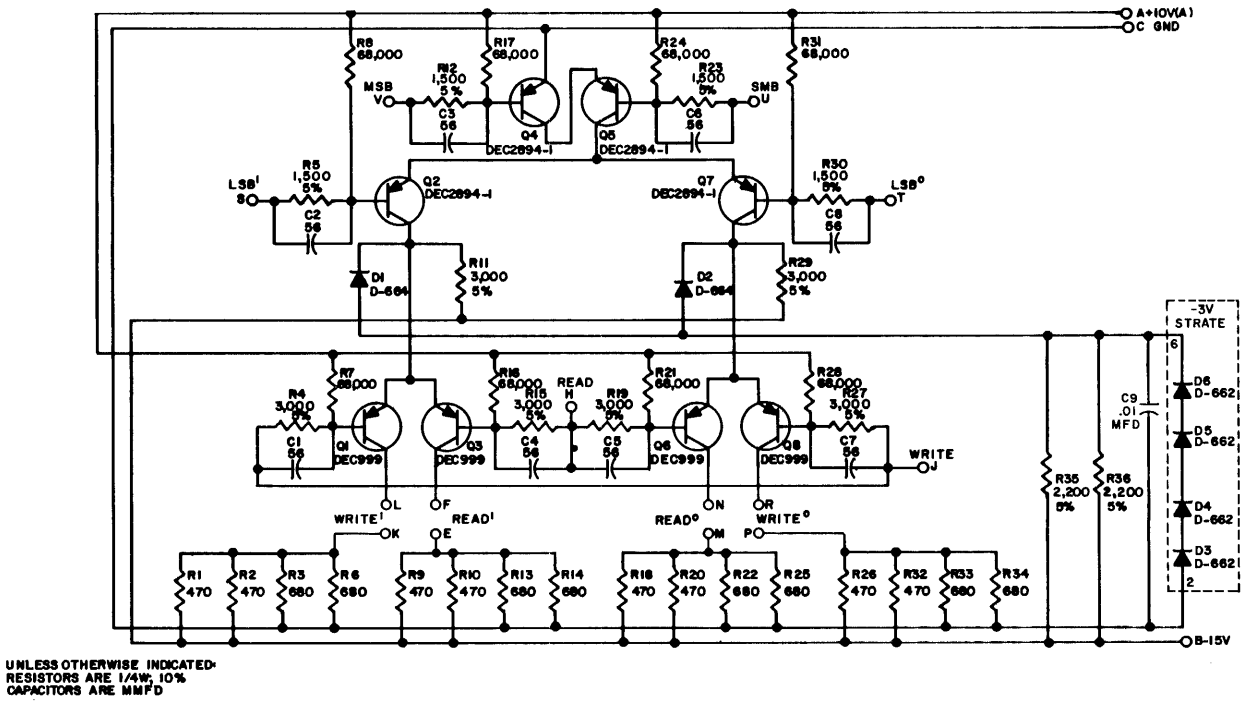
DC Sense Amplifier RS-C-G001



Master Slice Control RS-B-G002

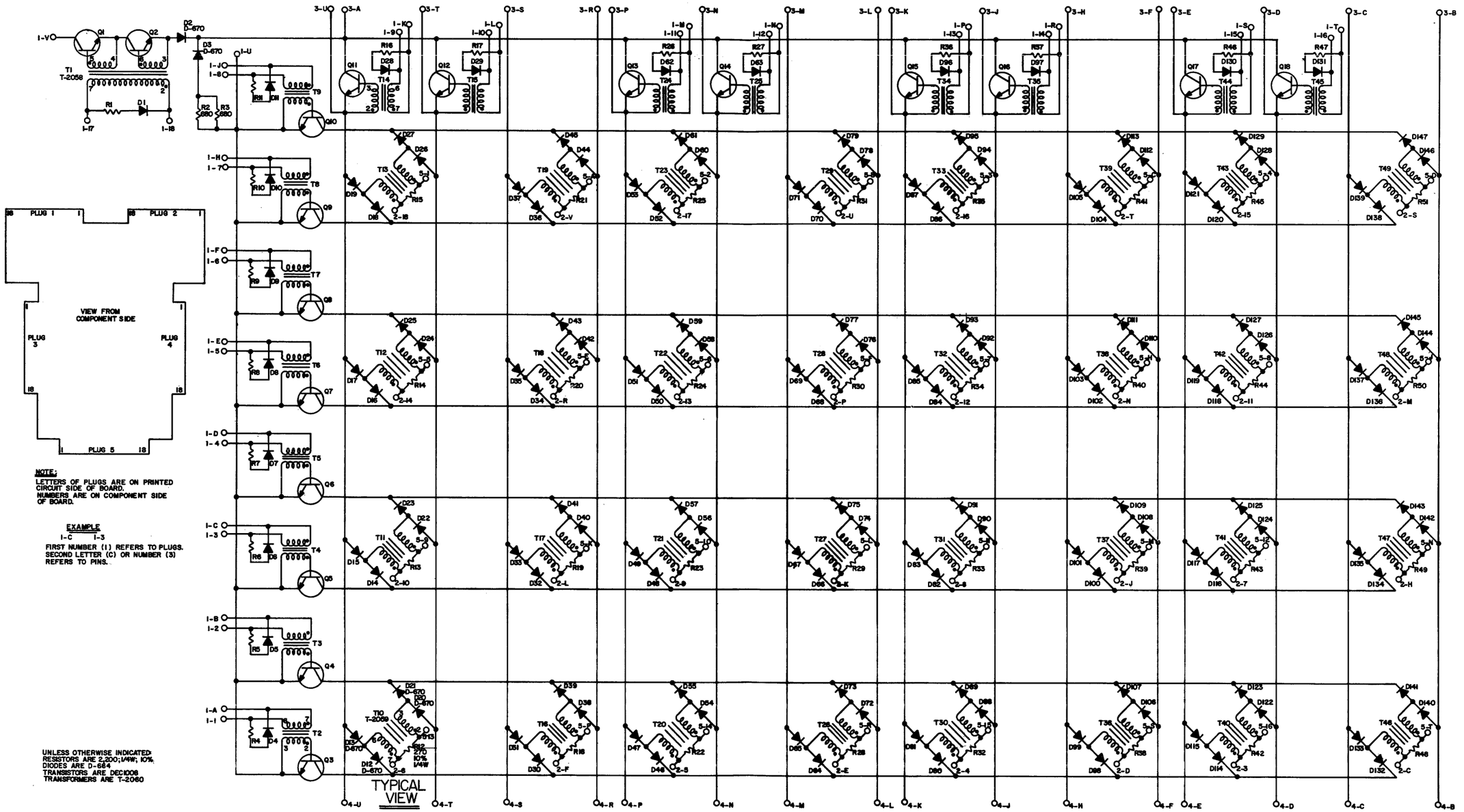


Inhibit Driver RS-B-G201



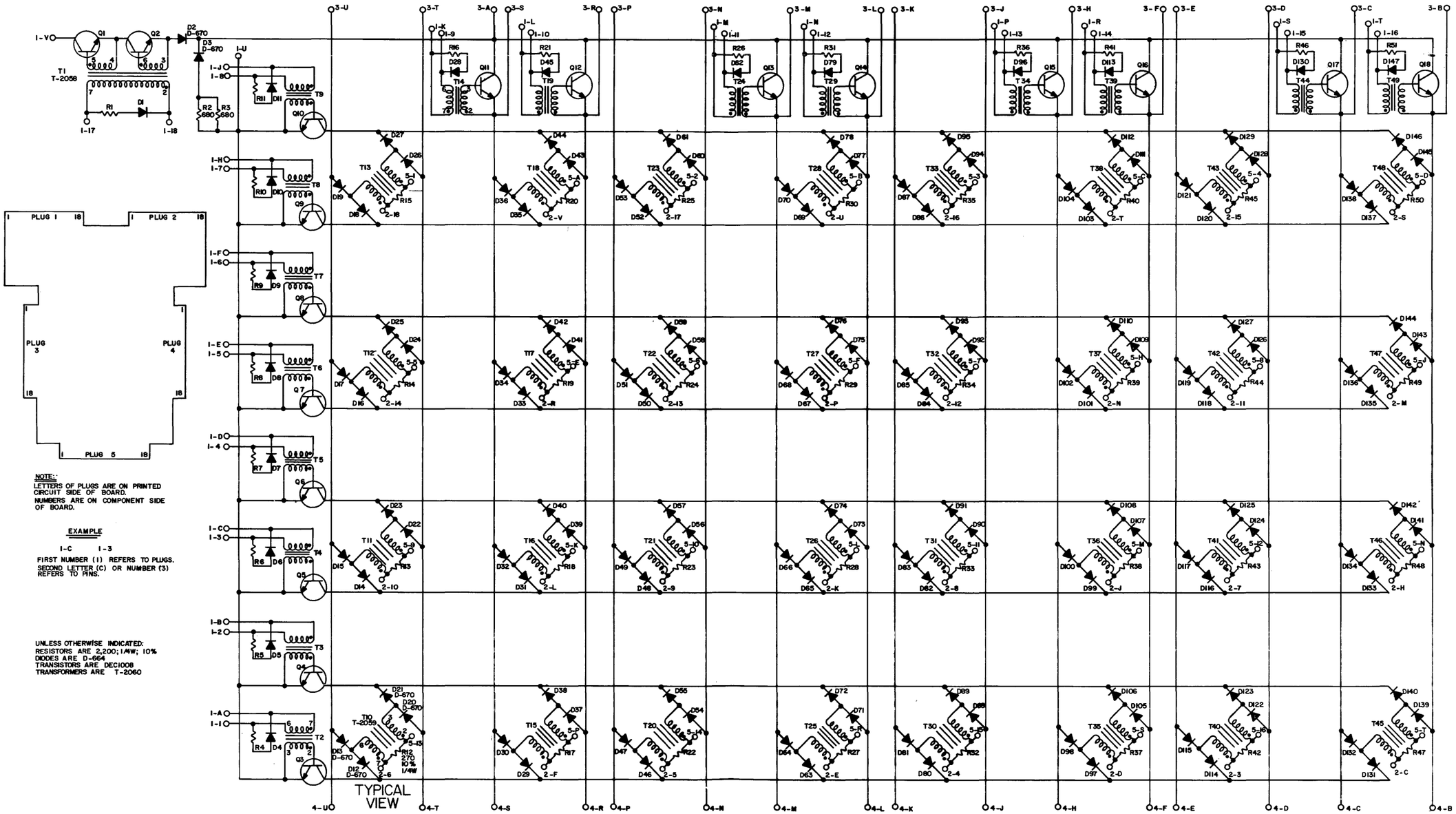
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W, 10%
CAPACITORS ARE MMFD

Memory Selector RS-B-G202



Memory Selector Matrix RS-D-G601

Memory Selector Matrix RS-D-G601



NOTE:
LETTERS OF PLUGS ARE ON PRINTED CIRCUIT SIDE OF BOARD.
NUMBERS ARE ON COMPONENT SIDE OF BOARD.

EXAMPLE

I-C I-3

FIRST NUMBER (1) REFERS TO PLUGS.
SECOND LETTER (C) OR NUMBER (3) REFERS TO PINS.

UNLESS OTHERWISE INDICATED:
RESISTORS ARE 2,200;1/4W; 10%
DIODES ARE D-664
TRANSISTORS ARE DEC1008
TRANSFORMERS ARE T-2060

Memory Selector Matrix RS-D-G602

Memory Selector Matrix RS-D-G602

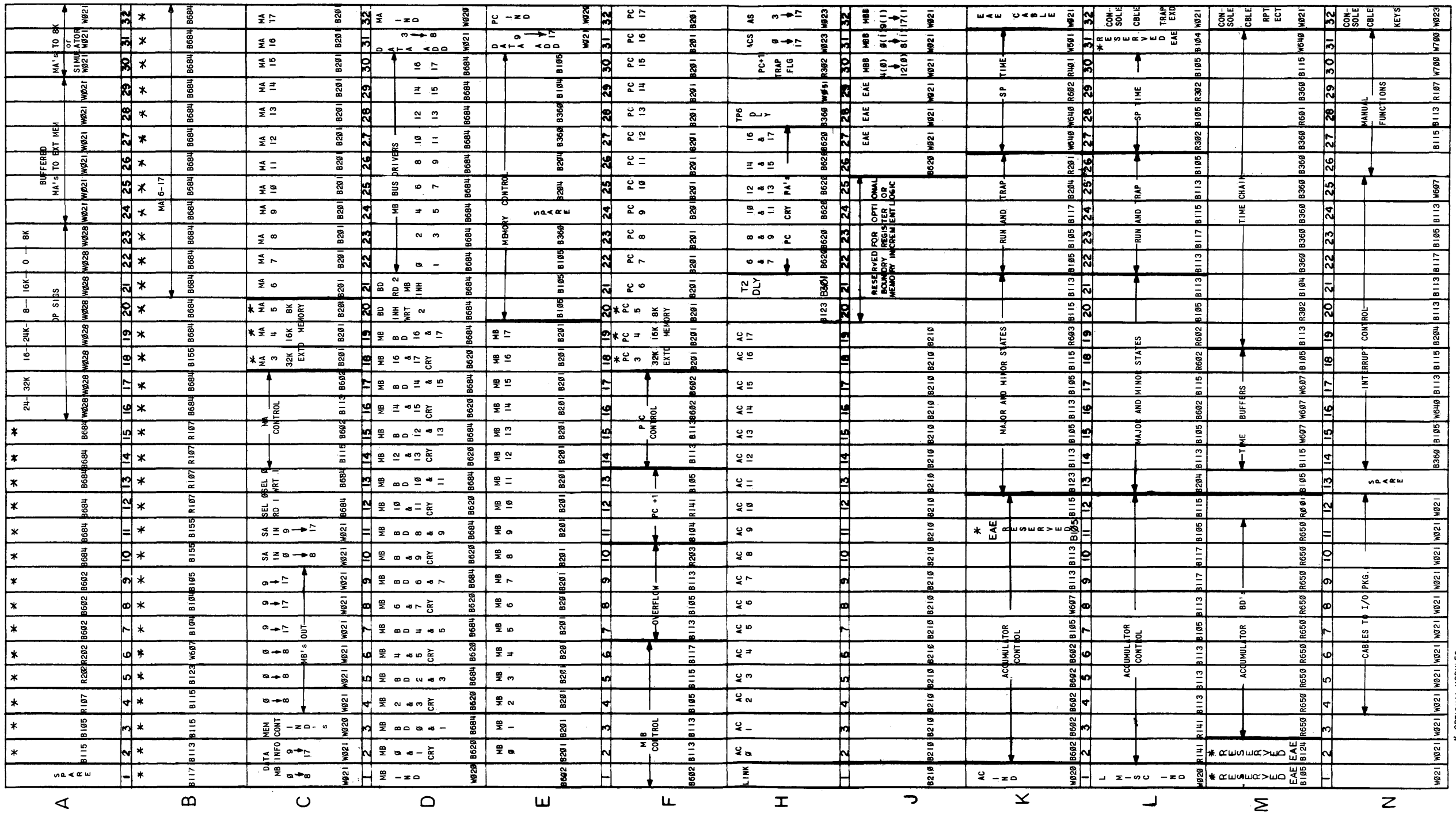
STANDARD MODULES	
TYPE	QUANTITY
B104	3
B105	23
B113	26
B115	12
B117	6
B123	1
B201	43
B204	5
B210	19
B301	1
B360	12
B602	12
B620	16
B684	22
R001	1
R107	1
R141	3
R203	1
R302	4
R401	1
R601	1
R602	3
R603	1
R650	9
W051	1
W501	1
W607	5
W640	4
W700	2

OPTIONAL MODULES		
OPTION	TYPE	QUANTITY
177 EAE	B104	1
	B105	2
	B123	1
	B124	1
EXTD MEMORY (SEE OPTION INSTALLMENT MODIFICATION SHEETS)	B104	2
	B105	2
	B113	1
	B115	3
	B117	1
	B123	1
	B155	3
	B201	6
	B602	3
	B684	22
	R107	5
	R202	2
	W607	1

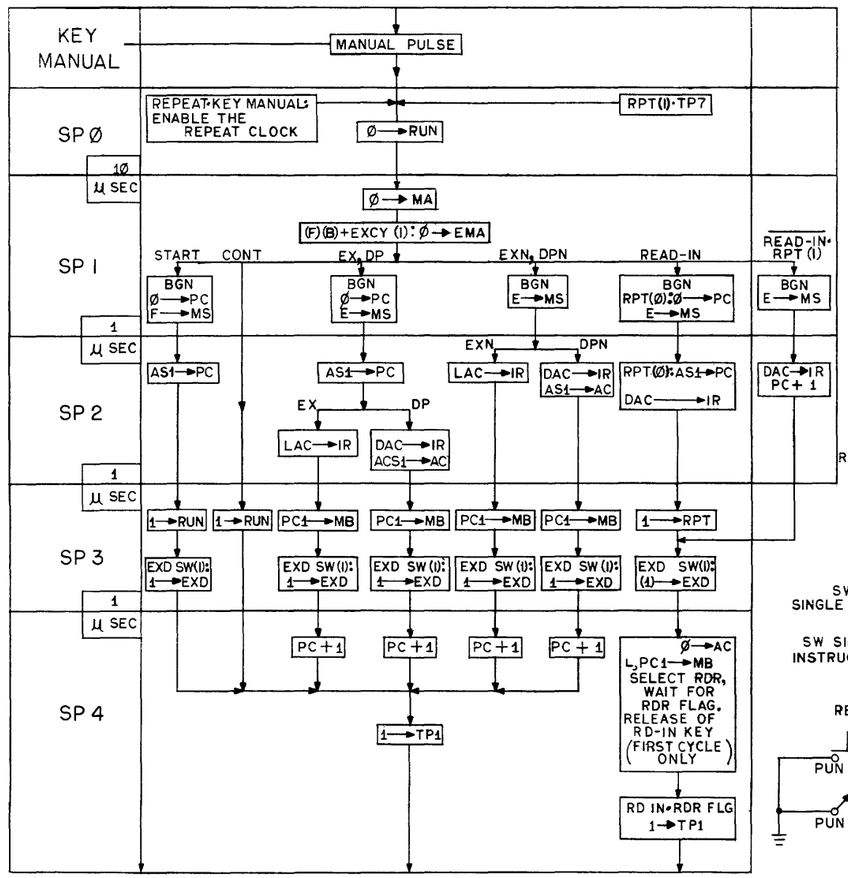
CP Module Map ML-D-KA77A-0-2

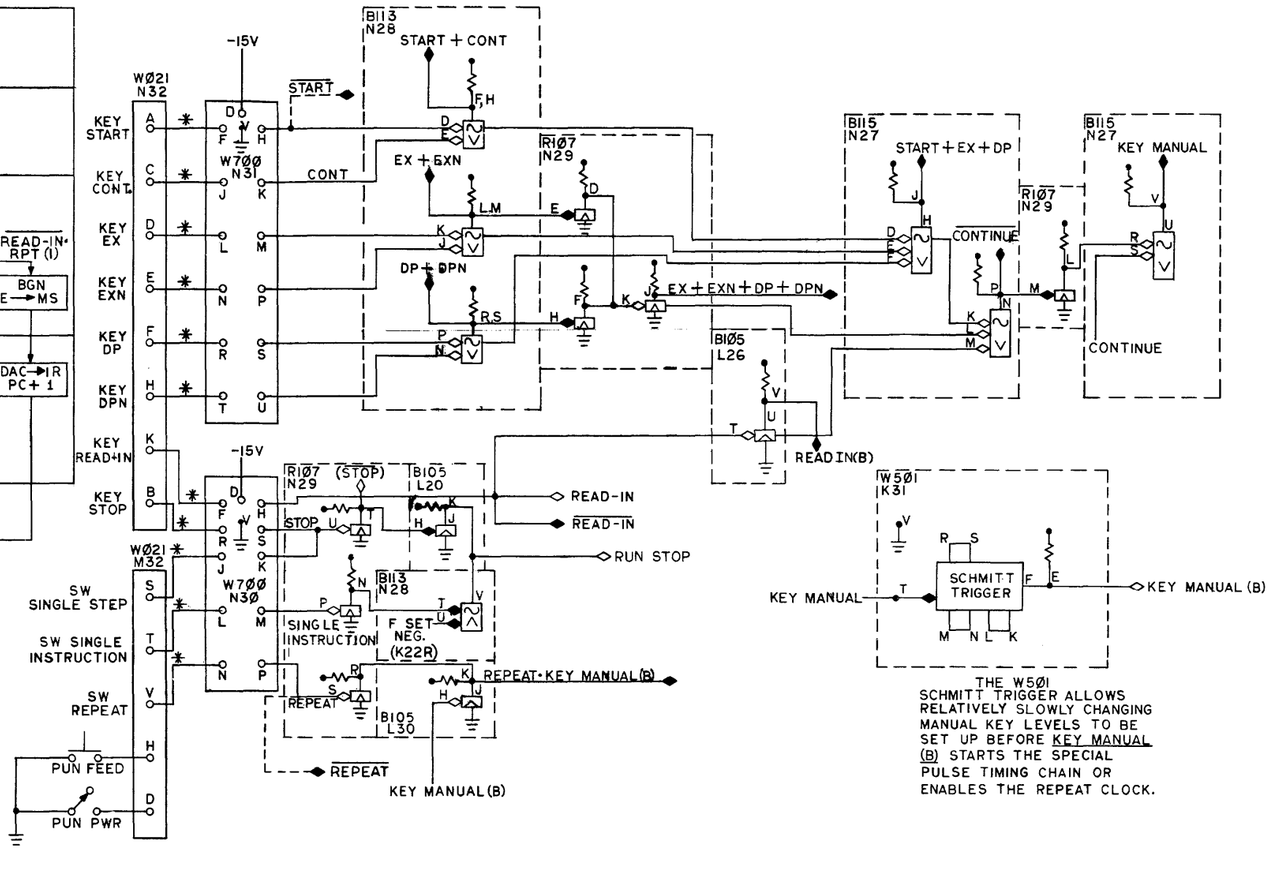
CP Module Map ML-D-KA77A-0-2

6-23a



CP Module Map ML-D-KA77A-0-2

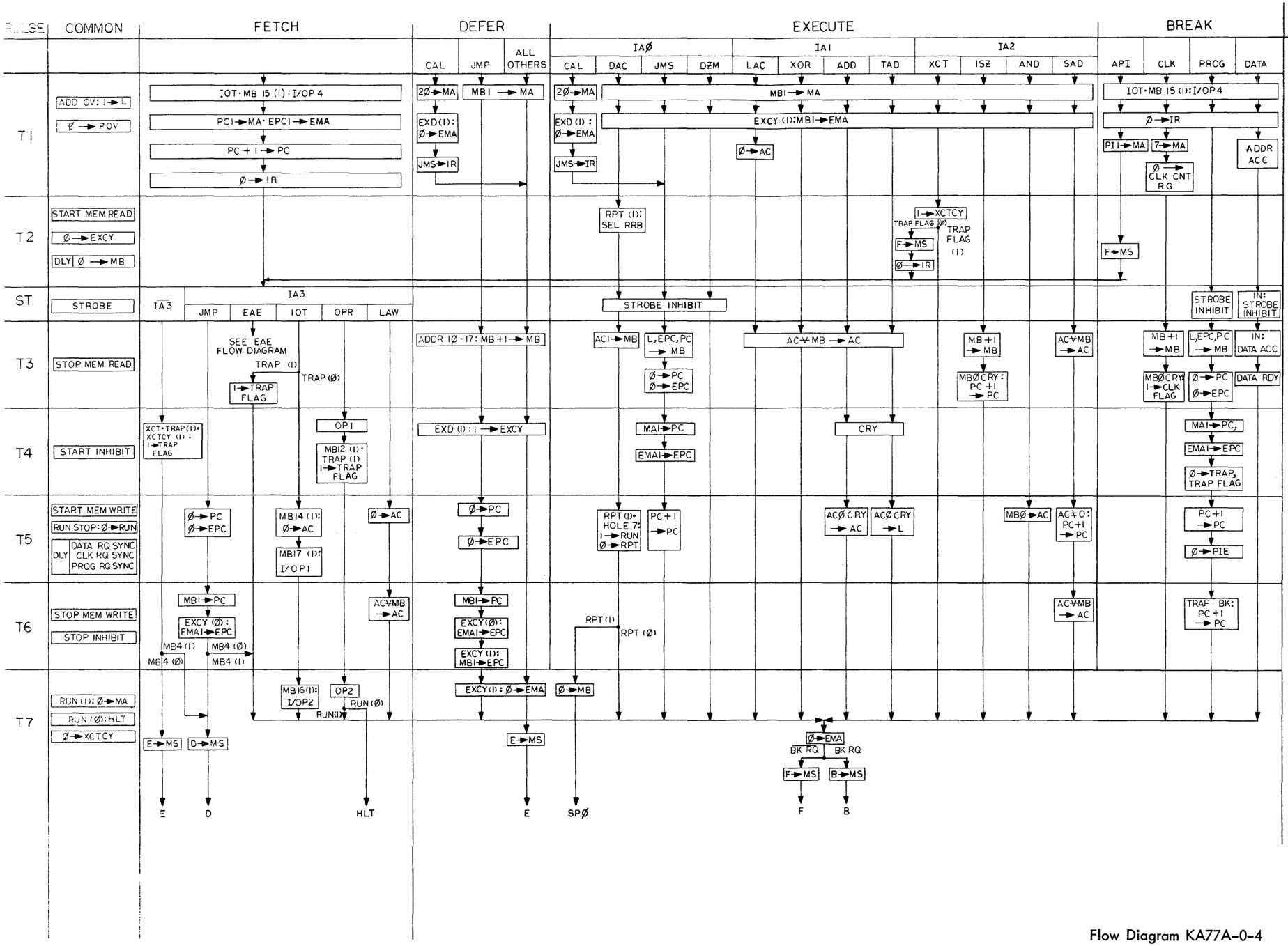




NOTE:	LEVELS FOR;	
	ASSERTION	NOT ASSERTION
*	+10V	GND
(DO NOT GND ANY OF THESE POINTS)		

BGN: GENERATED BY PWR CLK WHEN THE COMPUTER IS TURNED ON OR OFF.
GENERATED AT SP1 WHEN ANY MANUAL KEY IS OPERATED EXCEPT CONTINUE; (CONTINUE DOES NOT GENERATE BGN.)
FUNCTION CLEARS THE FOLLOWING REGISTERS AND/OR FLIP-FLOPS;
EXD, EXD SYNC, DBK, POV, MB, L, IR, AC, TRAP FLAG, I/O TRAP, RPT, XCT CY, PIE, DATA SYNC, CLK SYNC, PROG SYNC,
SETS THE EXCY TO A ONE (1).
FORCES THE EXECUTE CYCLE FOR ALL KEYS EXCEPT START. (AND CONTINUE).

NOTE: ALL PINS DESIGNATED BY ASTERICKS AND PIN D ON N30 ∧ N31 SHOULD BE COVERED WITH THE APPROPRIATELY COLORED SLEEVING.



NOTES

STROBE: SENSE AMPS TO THE MB, ALSO TO IR DURING FETCH.

OP1: OP SKIP EN ∀ MB8: PC+1→PC
MB5 (1): Ø→AC
MB6 (1): Ø→L
MB12 (1)·TRAP (Ø): Ø→RUN
MB7 (1)·MB13 (1): RAR
MB7 (1)·MB14 (1): RAL

OP2: MB13 (1): RAR
MB14 (1): RAL
MB15 (1): ACSI→AC
MB16 (1): $\overline{L}$→L
MB17 (1): $\overline{AC}$→AC

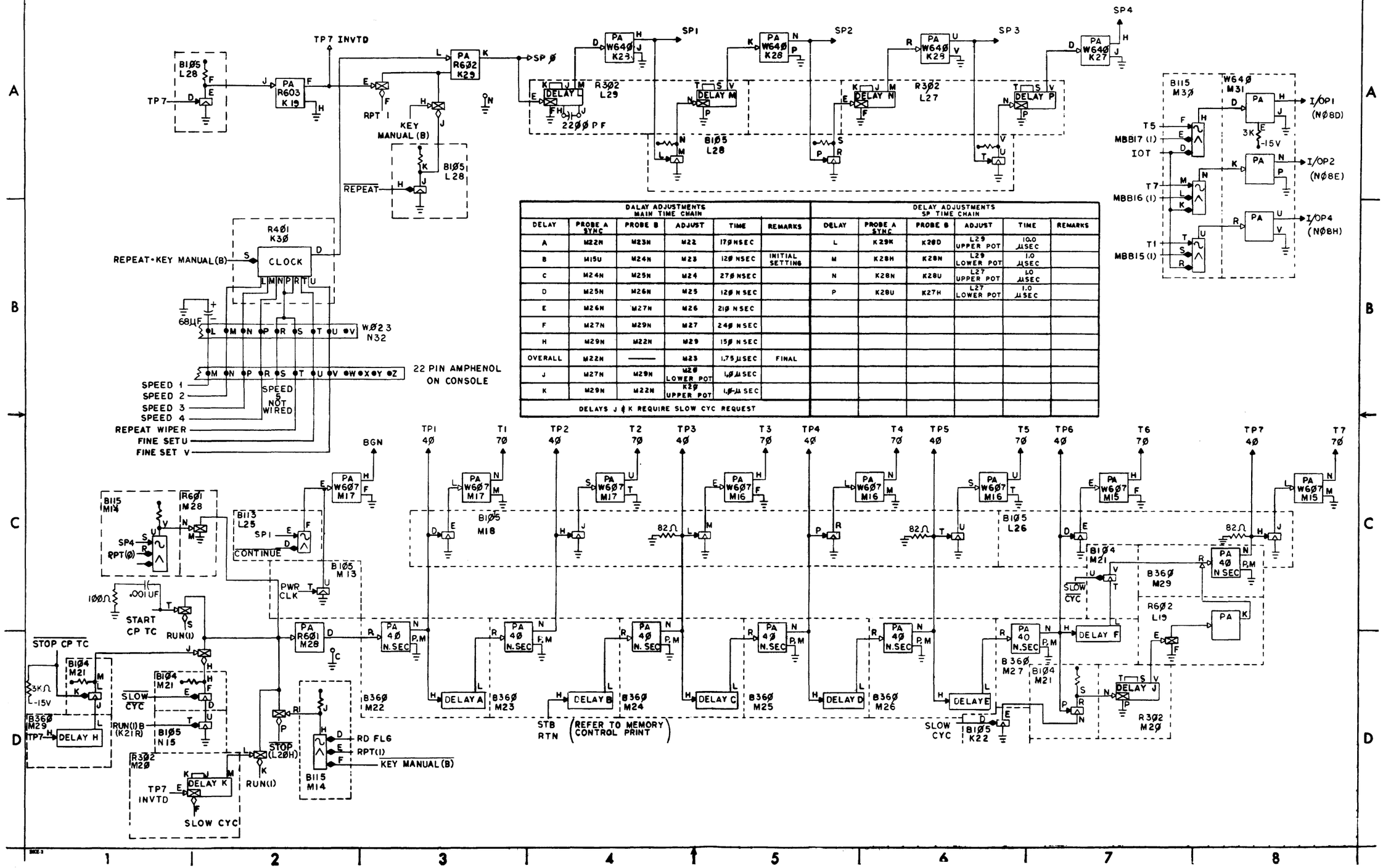
INST. DECODE

OCTAL	IA	IB	INST
ØØ	ØØ	ØØ	CAL
Ø4	ØØ	Ø1	DAC
1Ø	ØØ	1Ø	JMS
14	ØØ	11	DZM
2Ø	Ø1	ØØ	LAC
24	Ø1	Ø1	XOR
3Ø	Ø1	1Ø	ADD
34	Ø1	11	TAD
4Ø	1Ø	ØØ	XCT
44	1Ø	Ø1	ISZ
5Ø	1Ø	1Ø	AND
54	1Ø	11	SAD
6Ø	11	ØØ	JMP
64	11	Ø1	EAE
7Ø	11	1Ø	IOT
74	11	11	ØPR/LAW

STROBE INH
2 CYCLE (IA3)
MEMORY STROBE (IAØ)
1CYCLE (IA3)

Flow Diagram KA77A-0-4

Flow Diagram KA77A-0-4



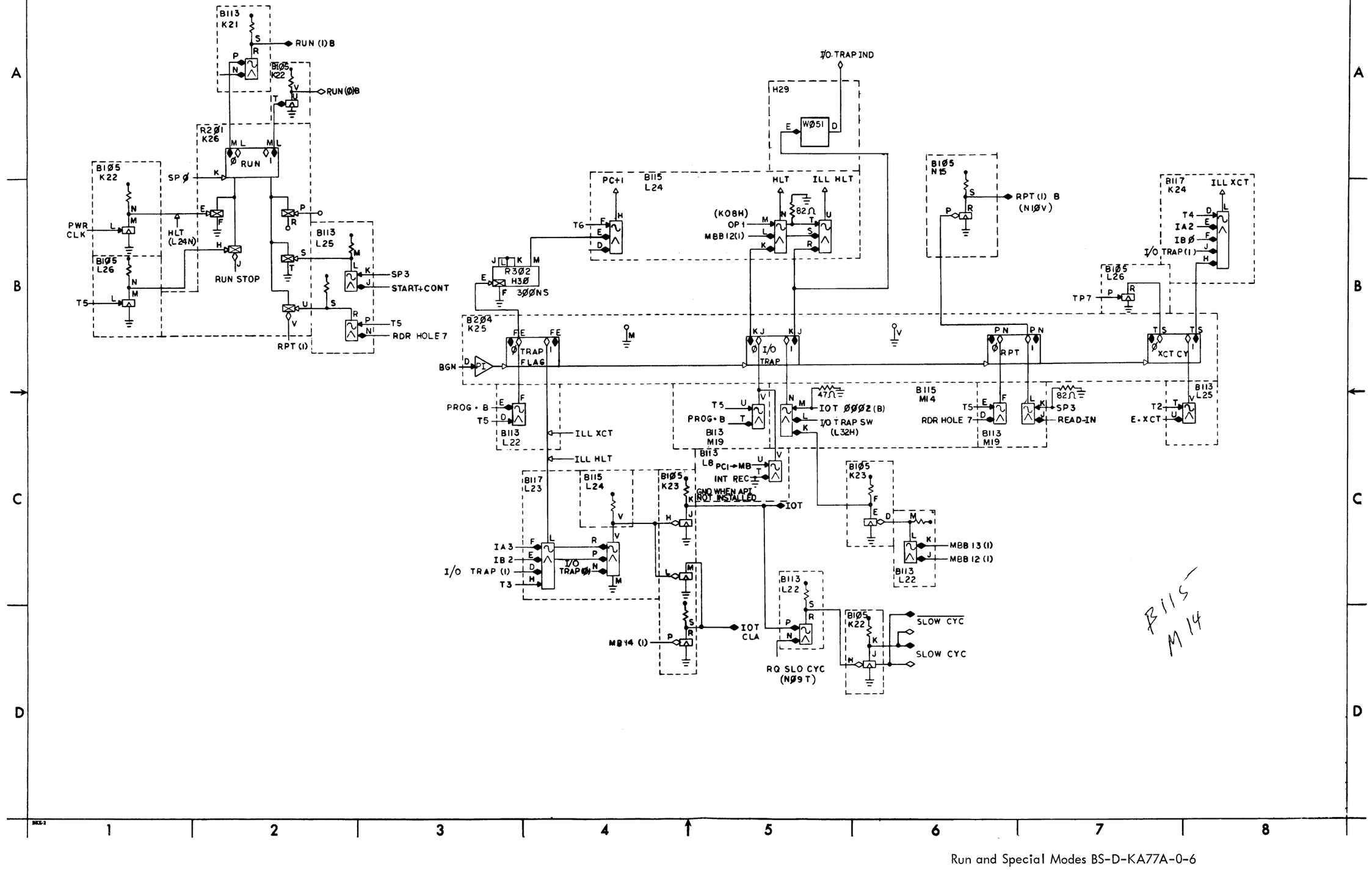
DALAY ADJUSTMENTS MAIN TIME CHAIN

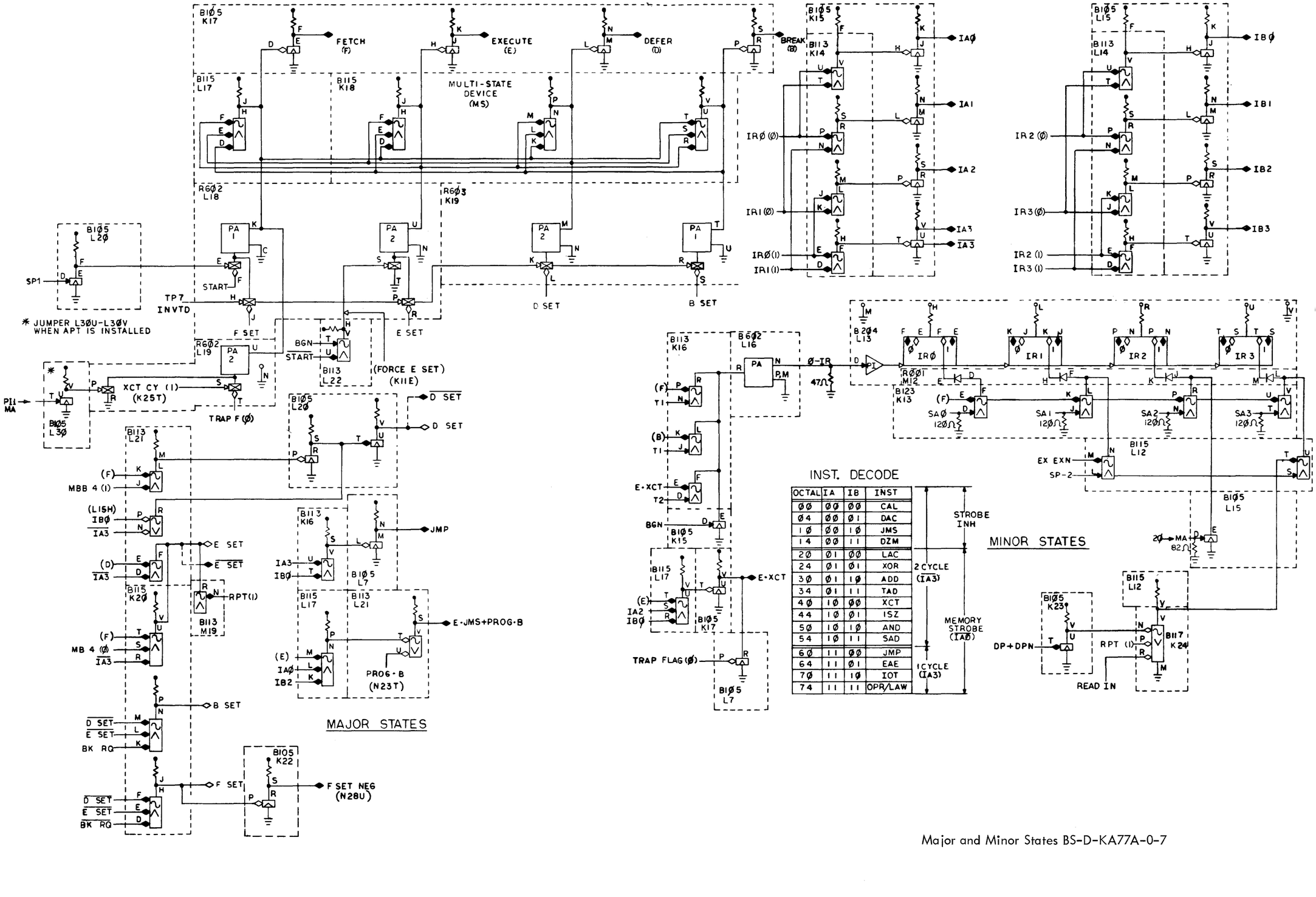
DELAY	PROBE A SYNC	PROBE B	ADJUST	TIME	REMARKS
A	M22N	M23N	M22	17ØNSEC	
B	M15U	M24N	M23	12Ø NSEC	INITIAL SETTING
C	M24N	M25N	M24	27Ø NSEC	
D	M25N	M26N	M25	12Ø N SEC	
E	M26N	M27N	M26	21Ø N SEC	
F	M27N	M29N	M27	24Ø N SEC	
H	M29N	M22N	M29	15Ø N SEC	
OVERALL	M22N	——	M23	1.75 µSEC	FINAL
J	M27N	M29N	M2Ø LOWER POT	1.Ø µSEC	
K	M29N	M22N	K2Ø UPPER POT	1.Ø µ SEC	
DELAYS J & K REQUIRE SLOW CYC REQUEST					

DELAY ADJUSTMENTS SP TIME CHAIN

DELAY	PROBE A SYNC	PROBE B	ADJUST	TIME	REMARKS
L	K29N	K28D	L29 UPPER POT	10.0 µSEC	
M	K28H	K28N	L29 LOWER POT	1.0 µSEC	
N	K28N	K28U	L27 UPPER POT	1.0 µSEC	
P	K28U	K27H	L27 LOWER POT	1.0 µSEC	

Timing BS-D-KA77A-0-5


B113 K21
RUN (I) B
B105 K22
RUN (Ø) B
R201 K26
RUN
SP Ø
B105 K22
PWR CLK
B105 L26
T5
HLT (L24N)
RUN STOP
RPT (I)
B113 L25
SP3
START+CONT
T5
RDR HOLE 7
I/O TRAP IND
H29
WØ51
PC+1
B115 L24
T6
R302 H3Ø
3ØØNS
HLT
ILL HLT
(KØ8H)
OP 1
MBB12(I)
82Ω
B105 N15
RPT (I) B
(NIØV)
B117 K24
ILL XCT
T4
IA2
IBØ
I/O TRAP (I)
B105 L26
TP7
B204 K25
TRAP FLAG
BGN
I/O TRAP
RPT
XCT CY
PROG • B
T5
B113 L22
ILL XCT
ILL HLT
T5
PROG • B
B113 M19
47Ω
IOT ØØØ2 (B)
I/O TRAP SW (L32H)
B115 MI4
T5
RDR HOLE 7
B113 M19
82Ω
SP3
READ-IN
T2
E • XCT
B113 L25
B113 L8
PCI → MB
INT REC
GND WHEN APT NOT INSTALLED
IOT
B117 L23
B115 L24
B105 K23
IA 3
IB 2
I/O TRAP (I)
T3
I/O TRAP (Ø)
MB14 (I)
IOT CLA
B113 L22
RQ SLO CYC (NØ9T)
B105 K23
MBB 13 (I)
MBB 12 (I)
B113 L22
B105 K22
SLOW CYC
SLOW CYC
B113 M14

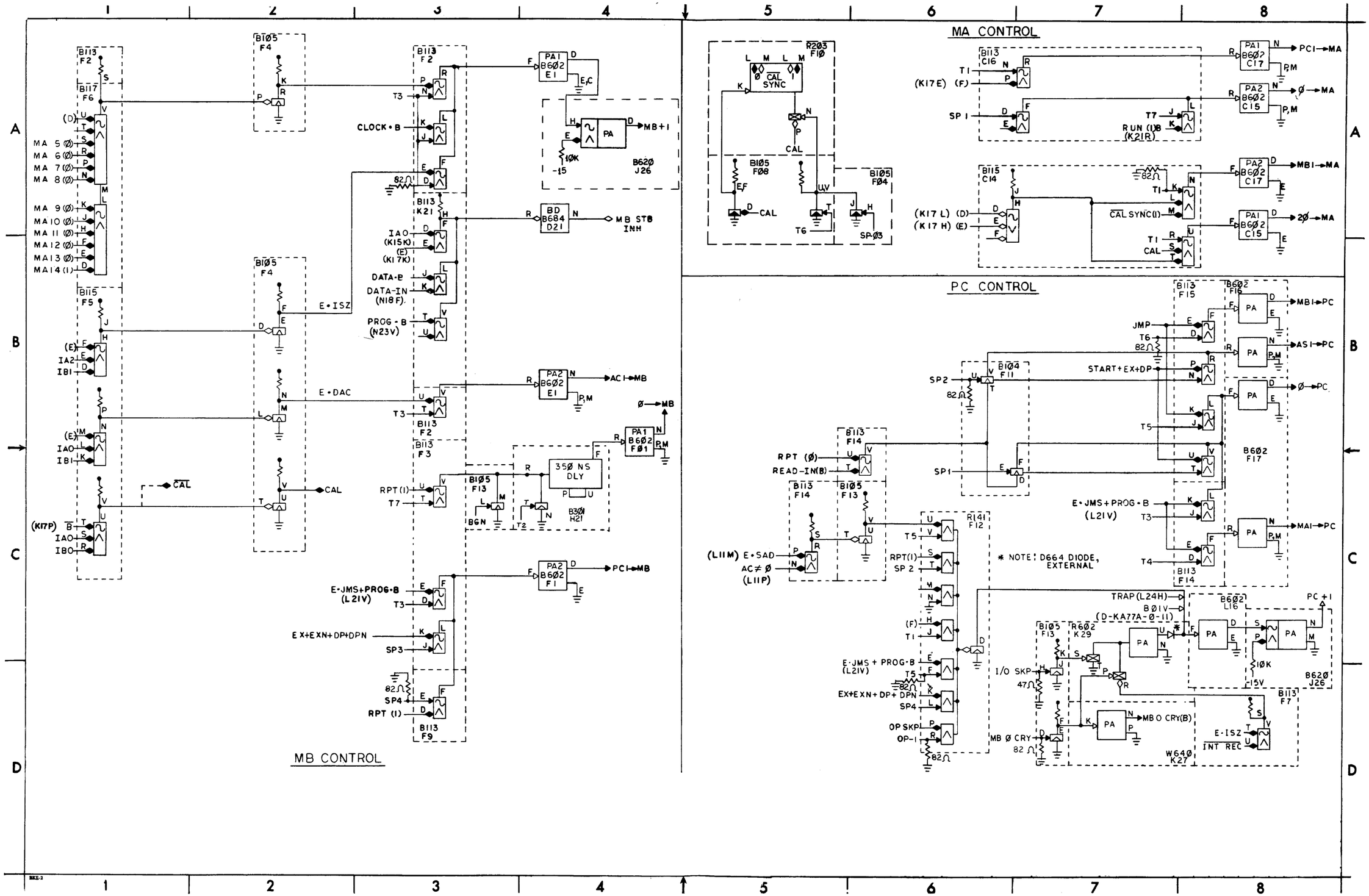


INST. DECODE

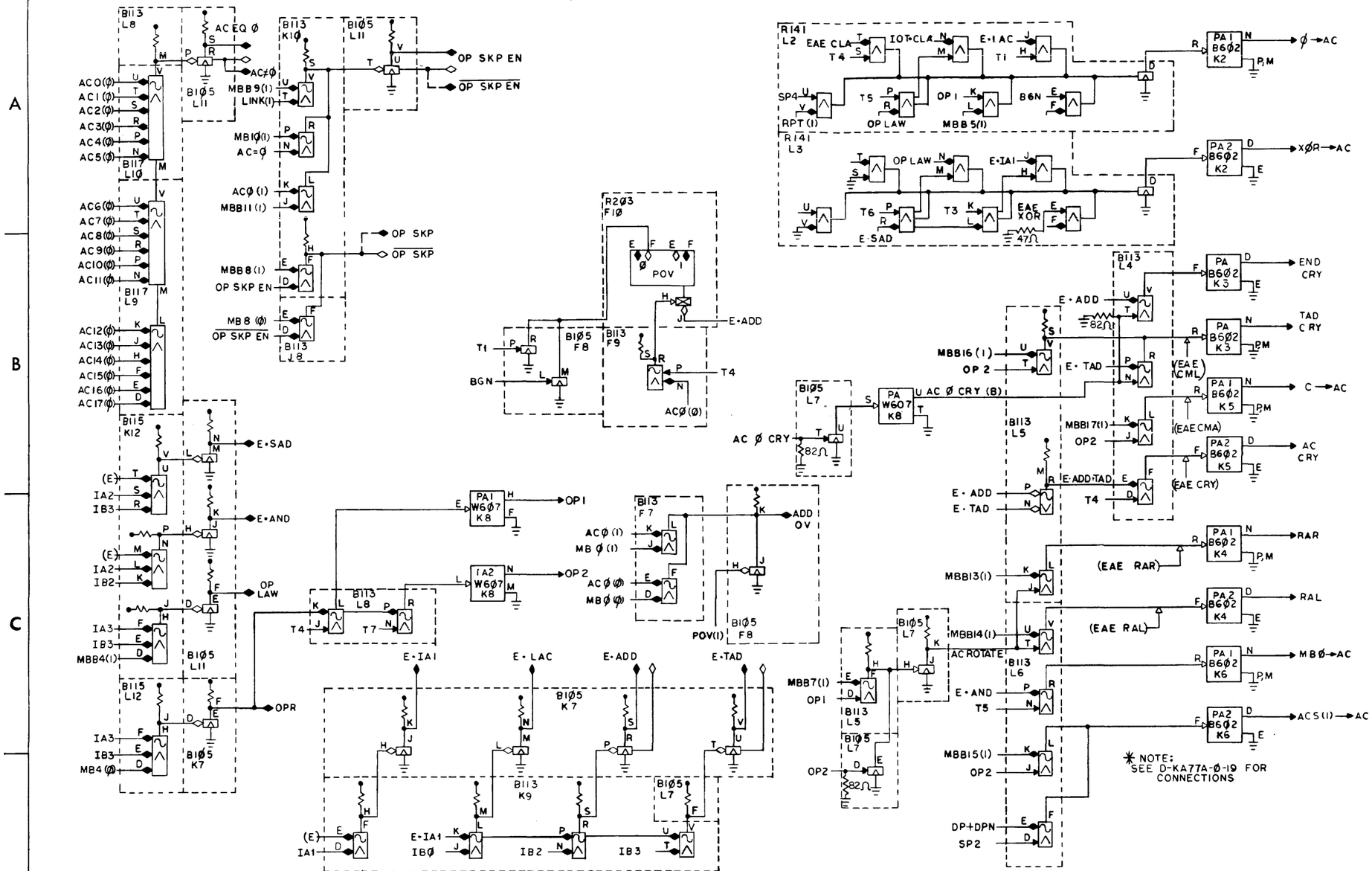
OCTAL	IA	IB	INST	
ØØ	ØØ	ØØ	CAL	STROBE INH
Ø4	ØØ	Ø1	DAC	
1Ø	ØØ	1Ø	JMS	
14	ØØ	11	DZM	
2Ø	Ø1	ØØ	LAC	2 CYCLE (IA3)
24	Ø1	Ø1	XOR	
3Ø	Ø1	1Ø	ADD	
34	Ø1	11	TAD	
4Ø	1Ø	ØØ	XCT	MEMORY STROBE (IAØ)
44	1Ø	Ø1	ISZ	
5Ø	1Ø	1Ø	AND	
54	1Ø	11	SAD	
6Ø	11	ØØ	JMP	1 CYCLE (IA3)
64	11	Ø1	EAE	
7Ø	11	1Ø	IOT	
74	11	11	OPR/LAW	

Major and Minor States BS-D-KA77A-0-7

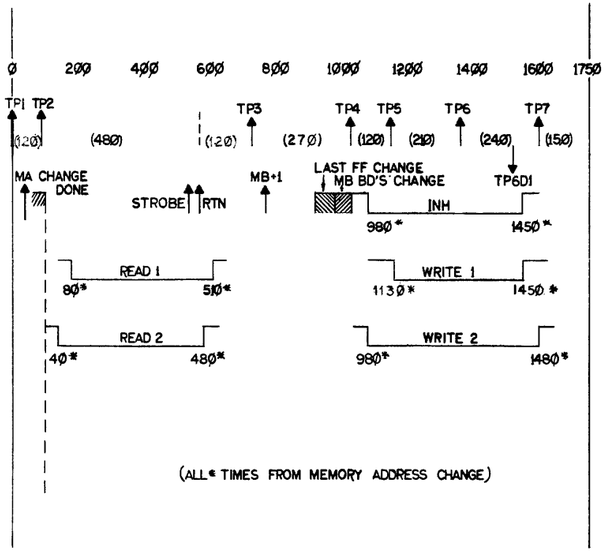
Major and Minor States BS-D-KA77A-0-7



MA, MB, and PC Control BS-D-KA77A-0-8



AC Control and Link BS-D-KA77A-0-9



(ALL * TIMES FROM MEMORY ADDRESS CHANGE)

MEMORY CONTROL TIMING

* DELAY ADJUSTMENT (SYNC ON PROBE 1)

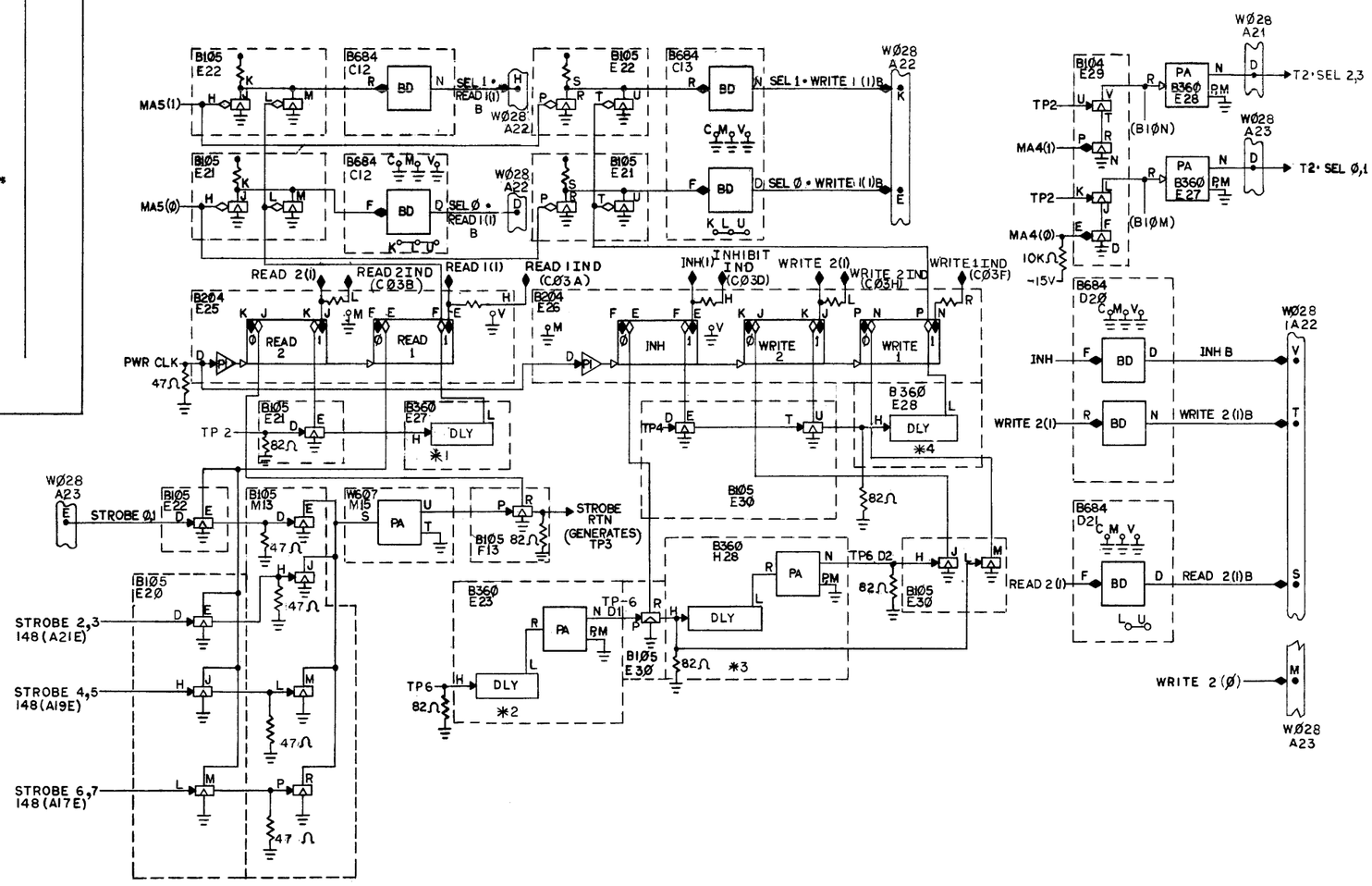
#	PROBE 1	PROBE 2	CONDITION
1	B30F	B31H	40 NS
2	B09F		470 NS
3	B31J	B30R	30NS(OFF)
4	B30R	B31J	150 NS (ON)

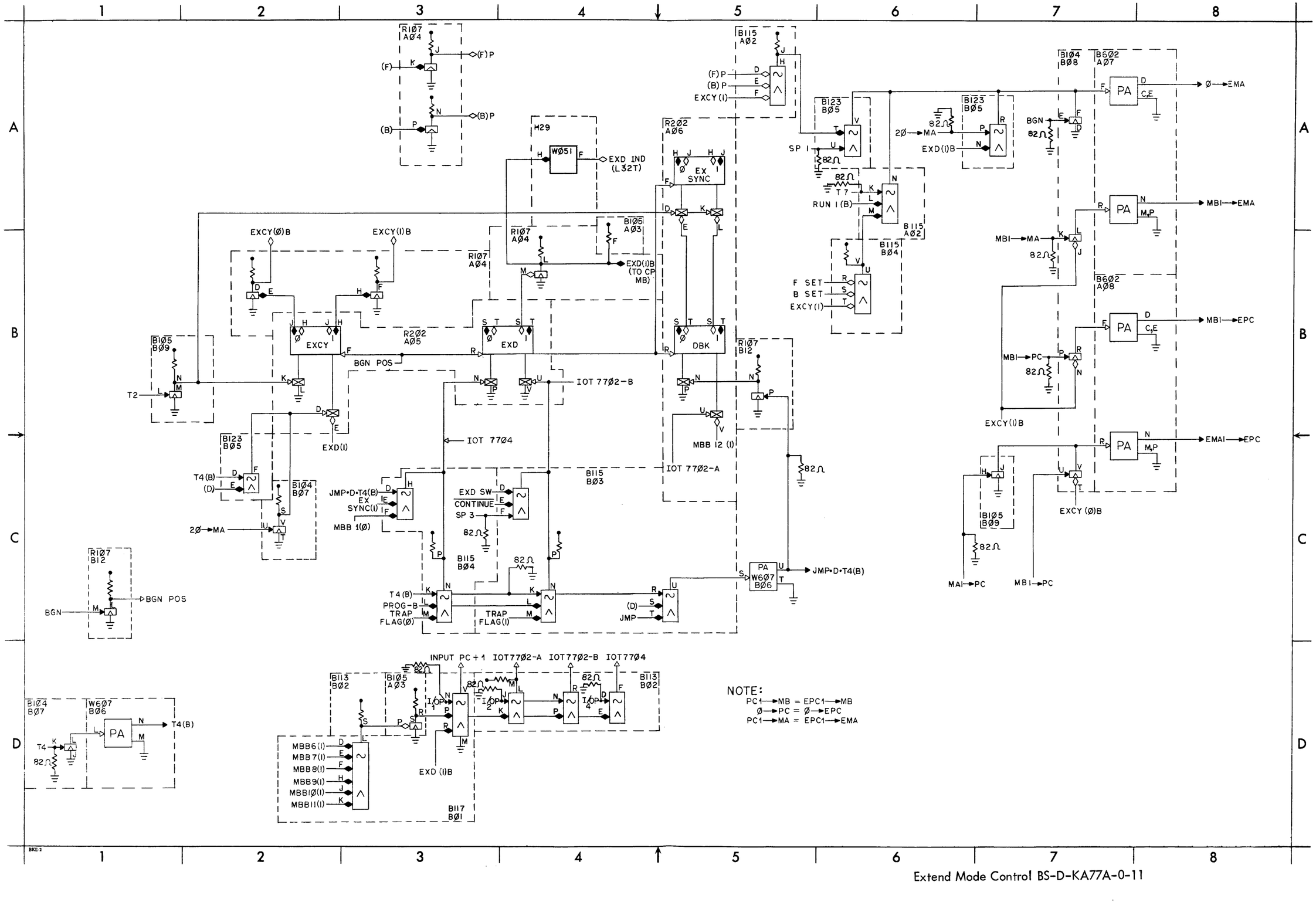
NOTE FOR AN 8K MEMORY

SEL Ø · READ 1(1) — B31H
SEL Ø · WRITE 1(1) — B31J
WRITE 2(1) ——— B30R
INHIBIT(1) ——— B09F
READ 2(1) ——— B30F

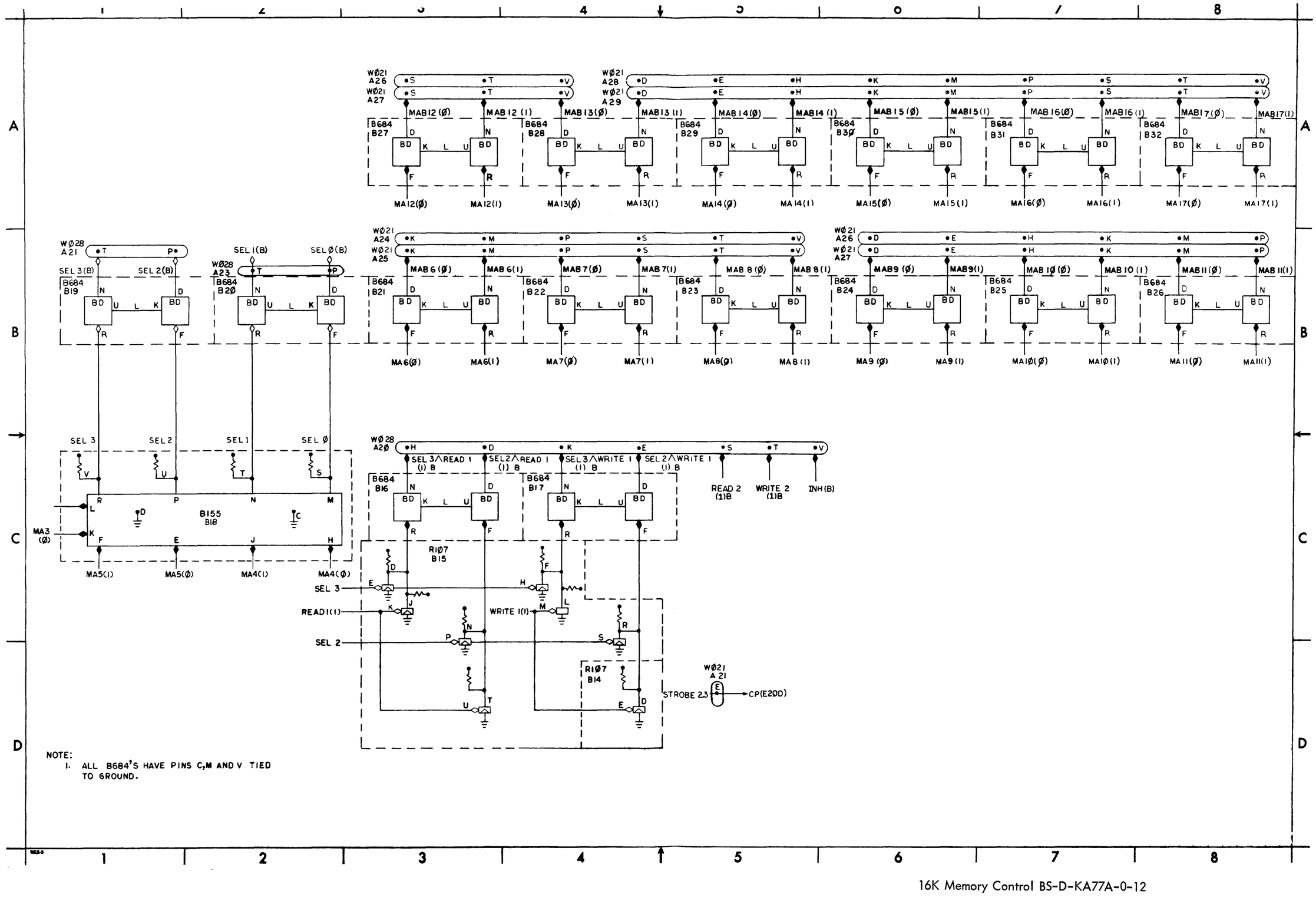
IF EXD OPTION NOT USED:
JUMPER: B18E — B20N
B18F — B20D

IF EXD OPTION USED:
REMOVE: B104 IN E29

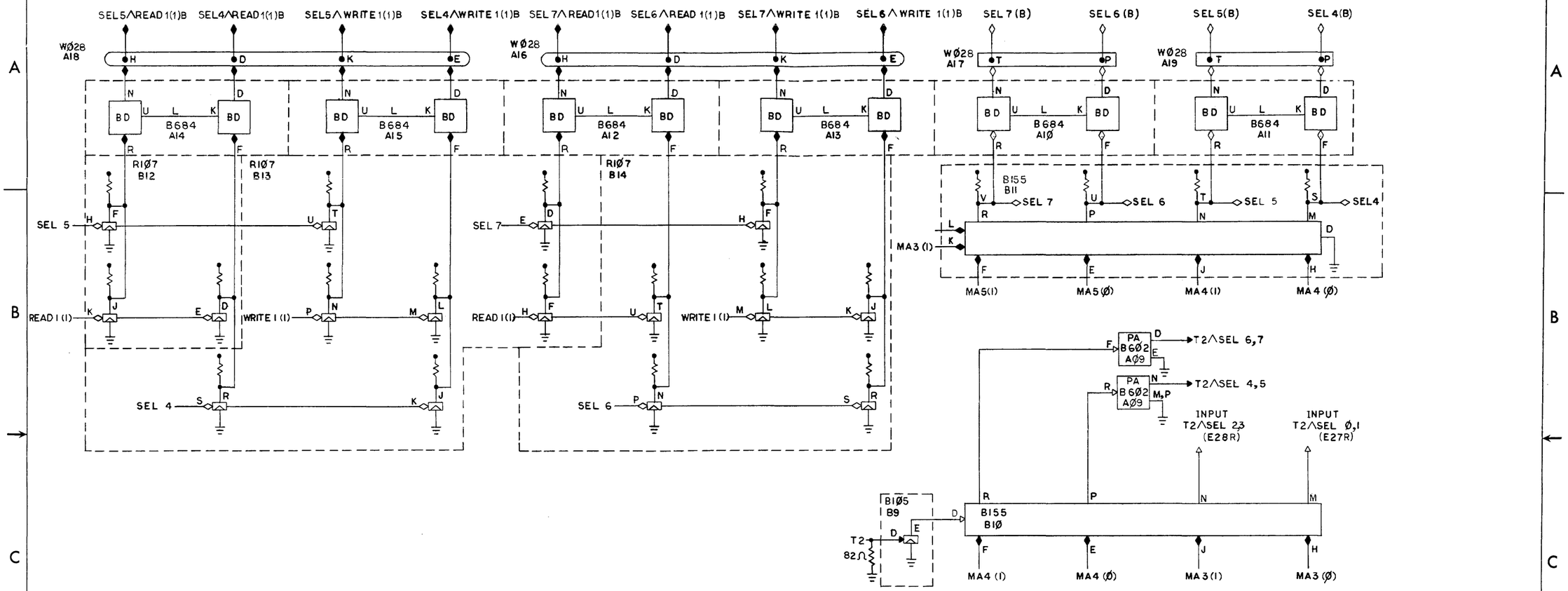




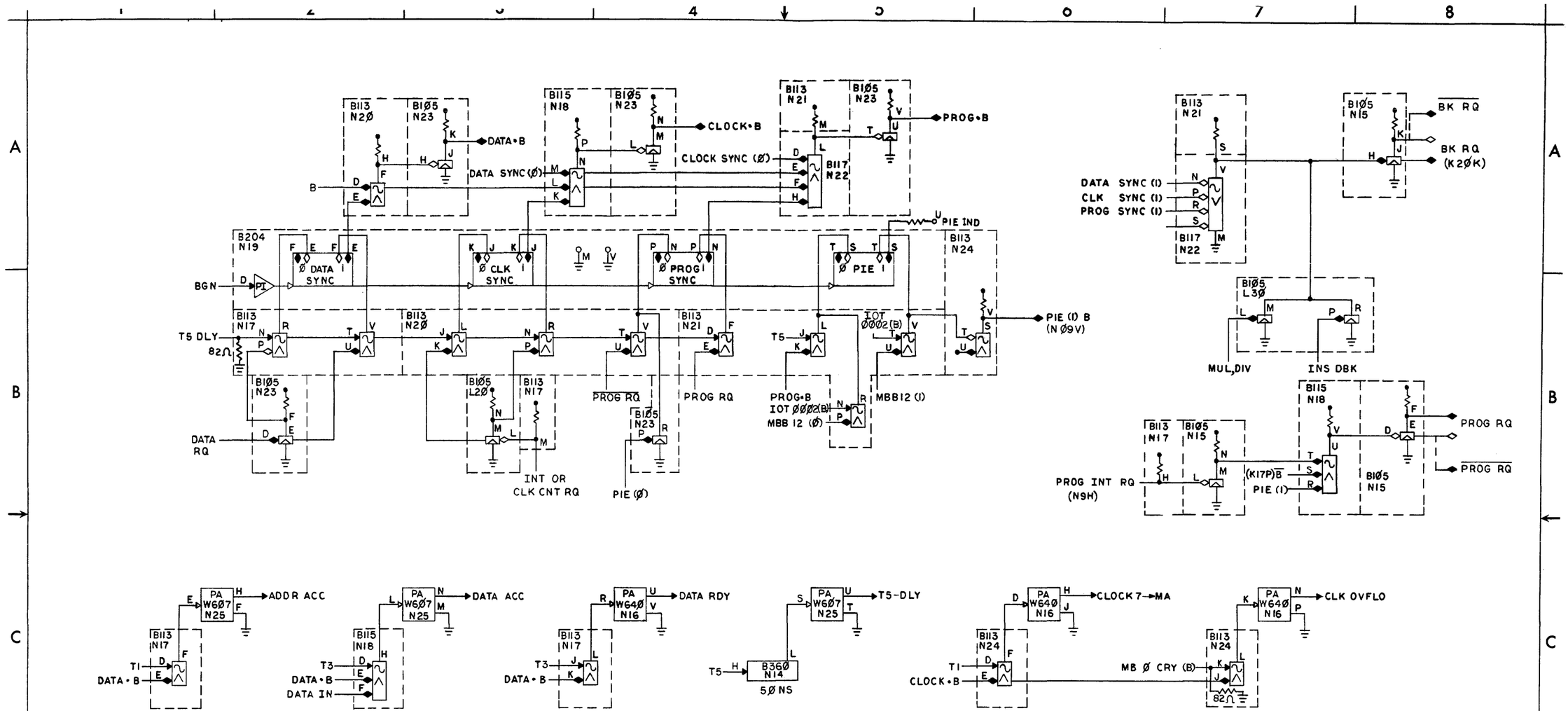
Extend Mode Control BS-D-KA77A-0-11

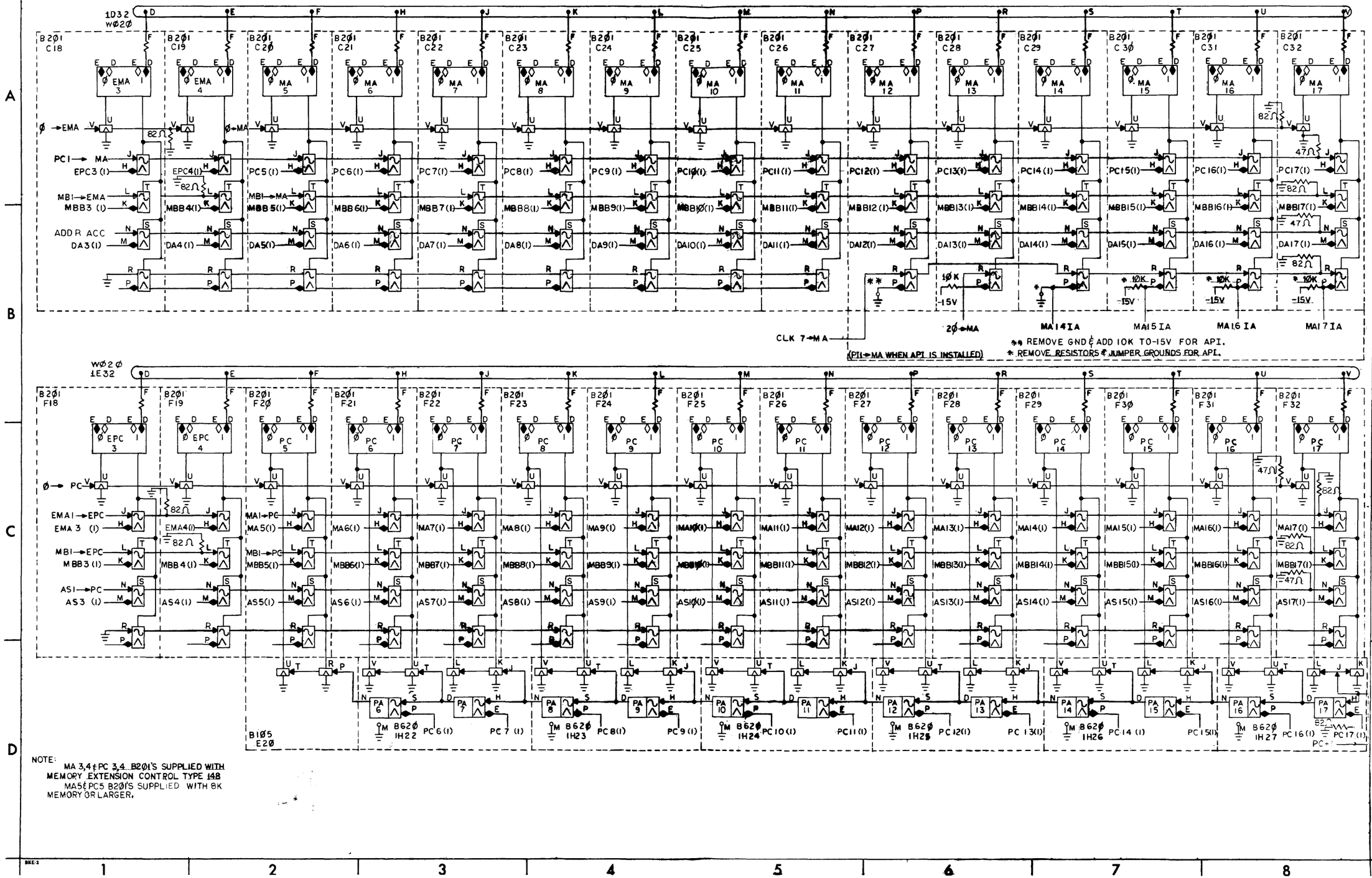


NOTE:
1. ALL B684'S HAVE PINS C,M AND V TIED TO GROUND.

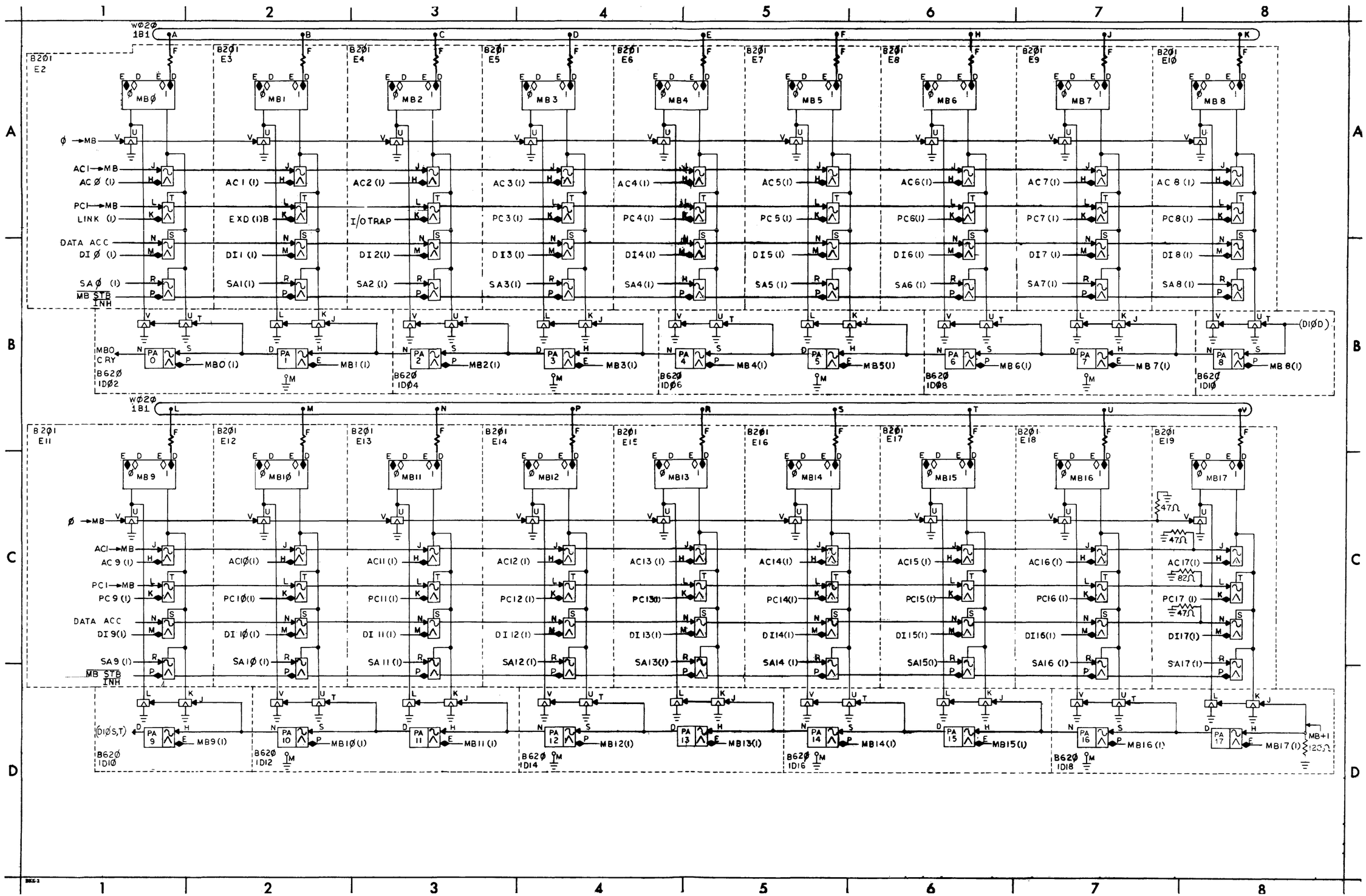


NOTE:
ALL B684'S HAVE PINS C,M AND V TIED TO GND.

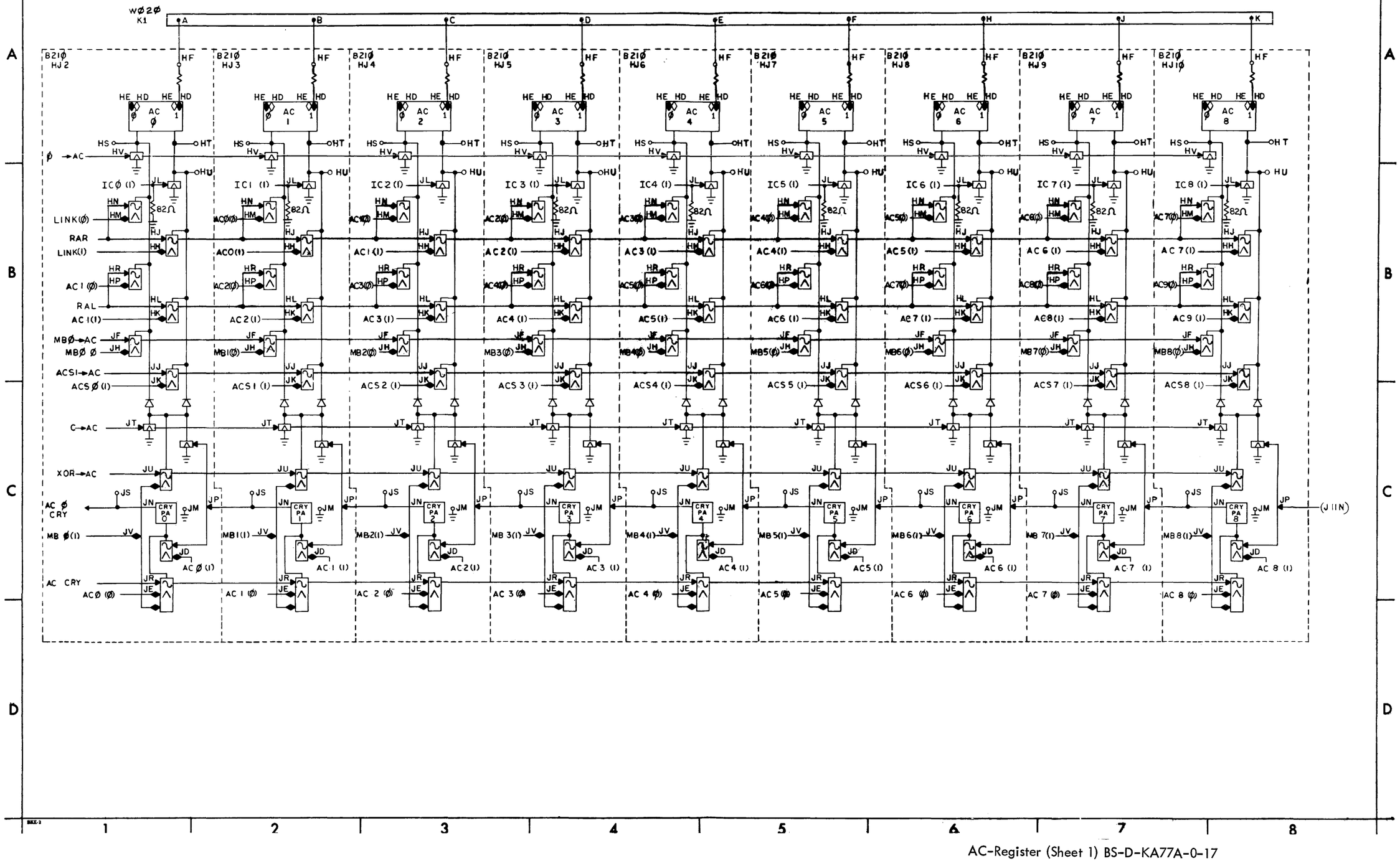

B113 N2Ø
BIØ5 N23
DATA•B
B115 N18
BIØ5 N23
CLOCK•B
DATA SYNC (Ø)
B113 N21
BIØ5 N23
PROG•B
CLOCK SYNC (Ø)
B117 N22
PIE IND
B204 N19
Ø DATA SYNC
Ø CLK SYNC
Ø PROG SYNC
Ø PIE
B113 N24
BGN
T5 DLY
82Ω
B113 N17
B113 N2Ø
B113 N21
T5
IOT ØØØ2(B)
PIE (I) B (N Ø9V)
BIØ5 N23
DATA RQ
BIØ5 L2Ø
B113 N17
INT OR CLK CNT RQ
PROG RQ
BIØ5 N23
PIE (Ø)
PROG RQ
PROG•B
IOT ØØØ2(B)
MBB 12 (Ø)
MBB12 (I)
B113 N21
BIØ5 N15
BK RQ
BK RQ (K2ØK)
DATA SYNC (I)
CLK SYNC (I)
PROG SYNC (I)
B117 N22
BIØ5 L3Ø
MUL,DIV
INS DBK
B115 N18
PROG RQ
PROG RQ
B113 N17
BIØ5 N15
PROG INT RQ (N9H)
(K17P)B
PIE (I)
BIØ5 N15
PA W6Ø7 N25
ADDR ACC
PA W6Ø7 N25
DATA ACC
PA W64Ø N16
DATA RDY
PA W6Ø7 N25
T5-DLY
B113 N17
T1
DATA•B
B115 N18
T3
DATA•B
DATA IN
B113 N17
T3
DATA•B
B36Ø N14
5Ø NS
T5
B113 N24
T1
CLOCK•B
PA W64Ø N16
CLOCK 7→MA
MB Ø CRY (B)
B113 N24
82Ω
PA W64Ø N16
CLK OVFLO



NOTE:
MA 3,4 & PC 3,4 B2Ø1'S SUPPLIED WITH MEMORY EXTENSION CONTROL TYPE 148
MA5 & PC5 B2Ø1'S SUPPLIED WITH 8K MEMORY OR LARGER.

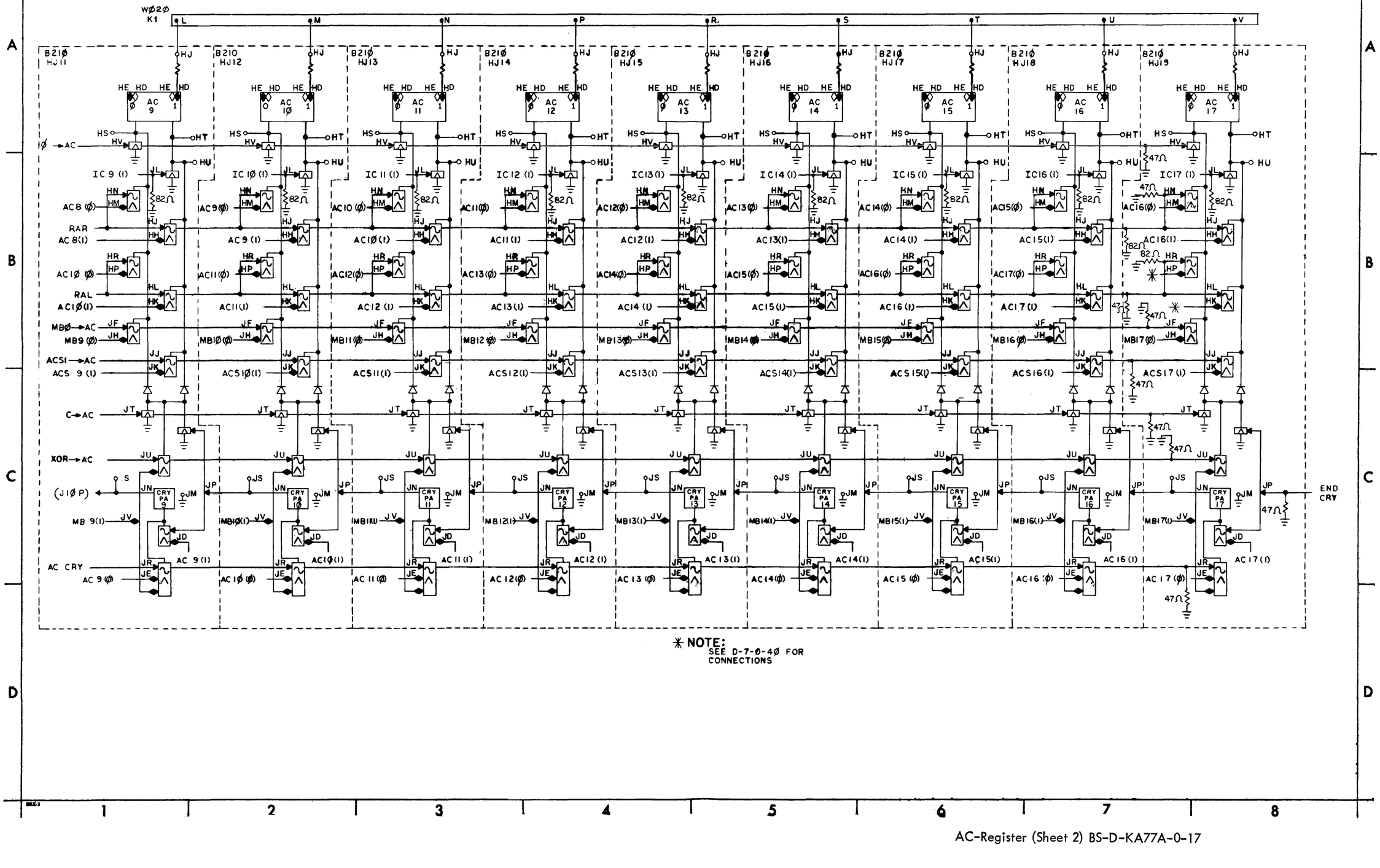


MB Registers BS-D-KA77A-0-16



AC-Register (Sheet 1) BS-D-KA77A-0-17

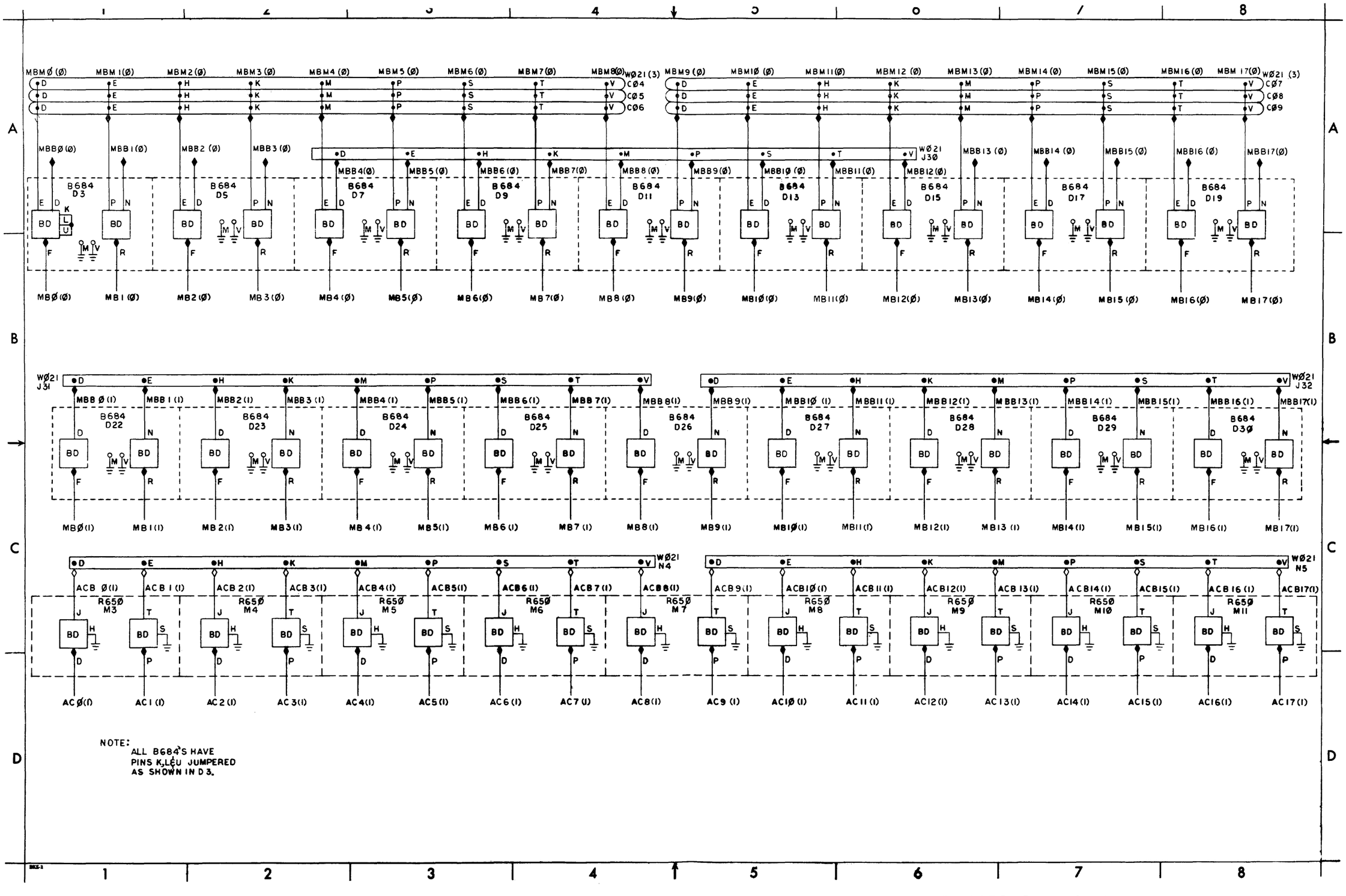
AC-Register (Sheet 1) BS-D-KA77A-0-17



✳ NOTE:
SEE D-7-Ø-4Ø FOR CONNECTIONS

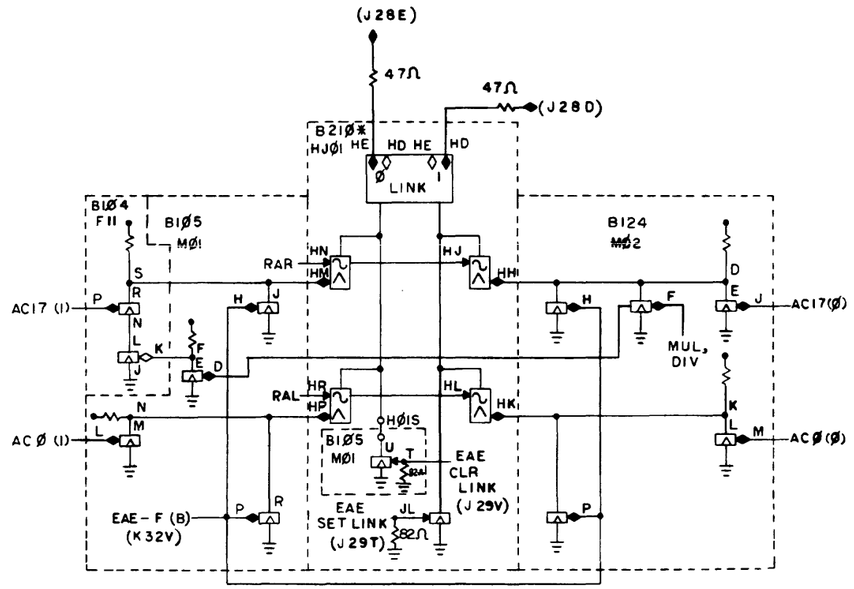
AC-Register (Sheet 2) BS-D-KA77A-0-17

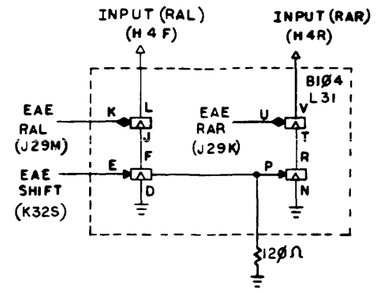
AC-Register (Sheet 2) BS-D-KA77A-0-17

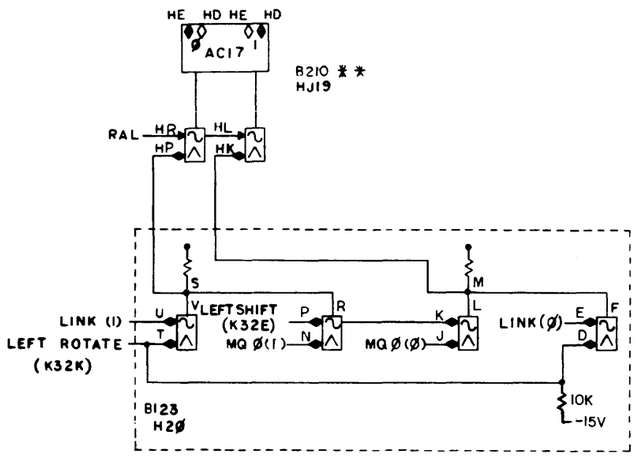


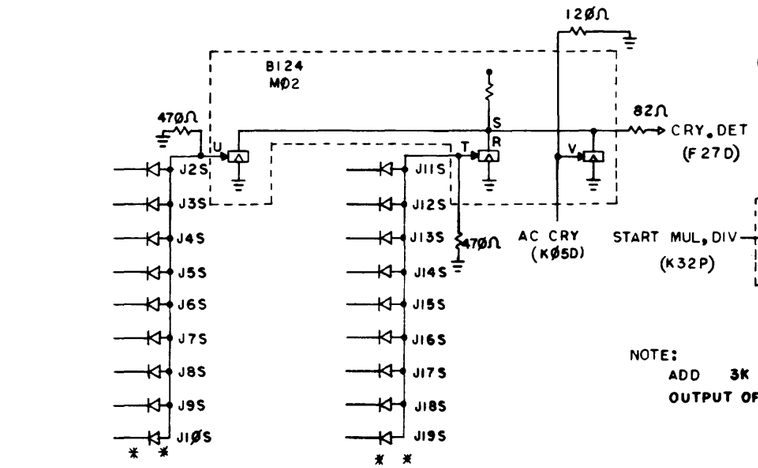
NOTE:
ALL B684'S HAVE
PINS K,L&U JUMPERED
AS SHOWN IN D3.

MB and AC Bus Drivers BS-D-KA77A-0-18

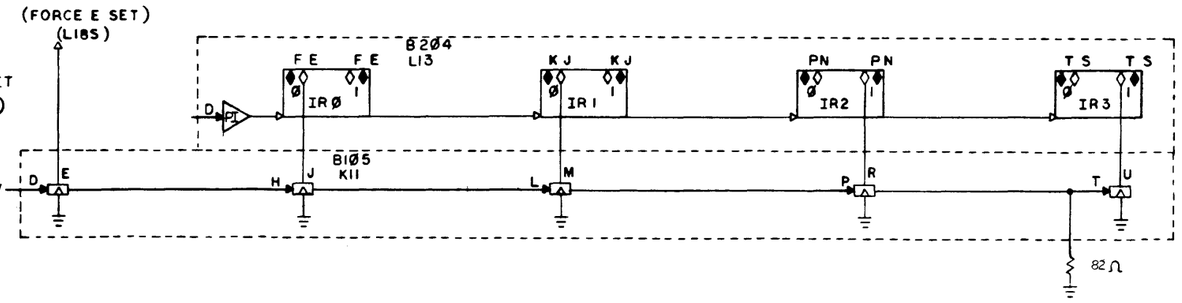






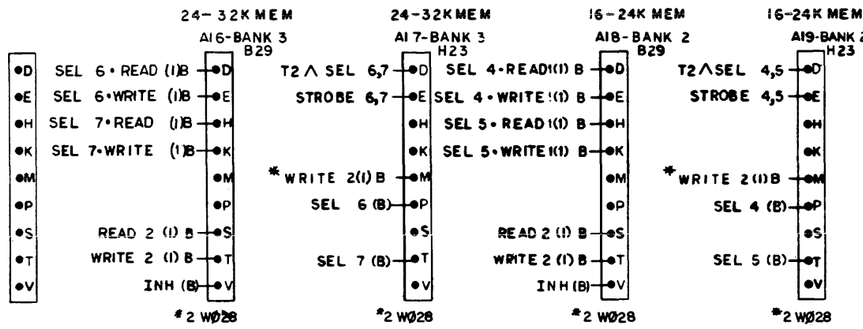


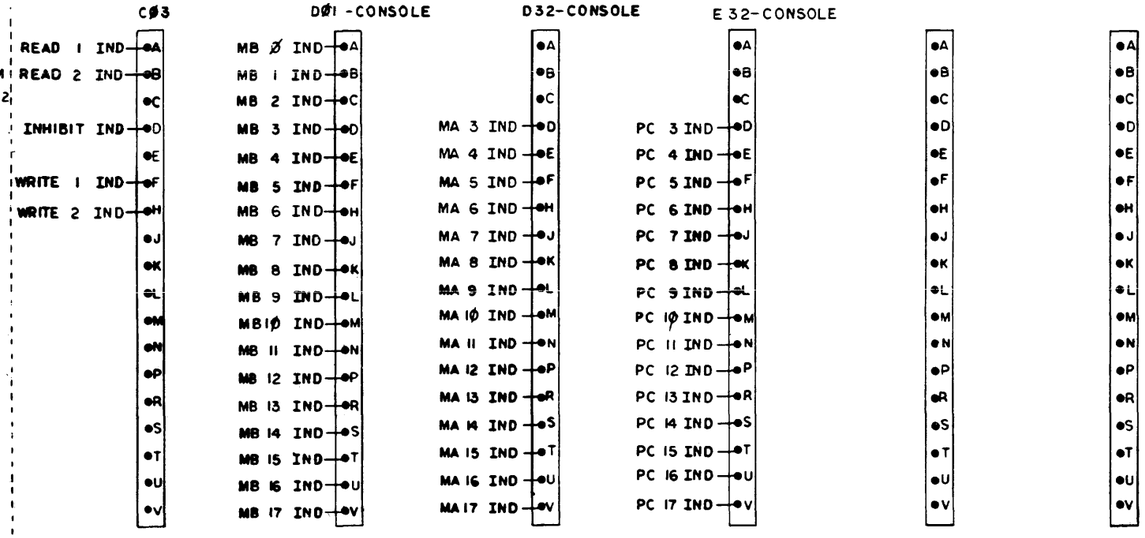
NOTE:
* SEE DWG. D-KA77A-0-9
** SEE DWG. D-KA77-0-17



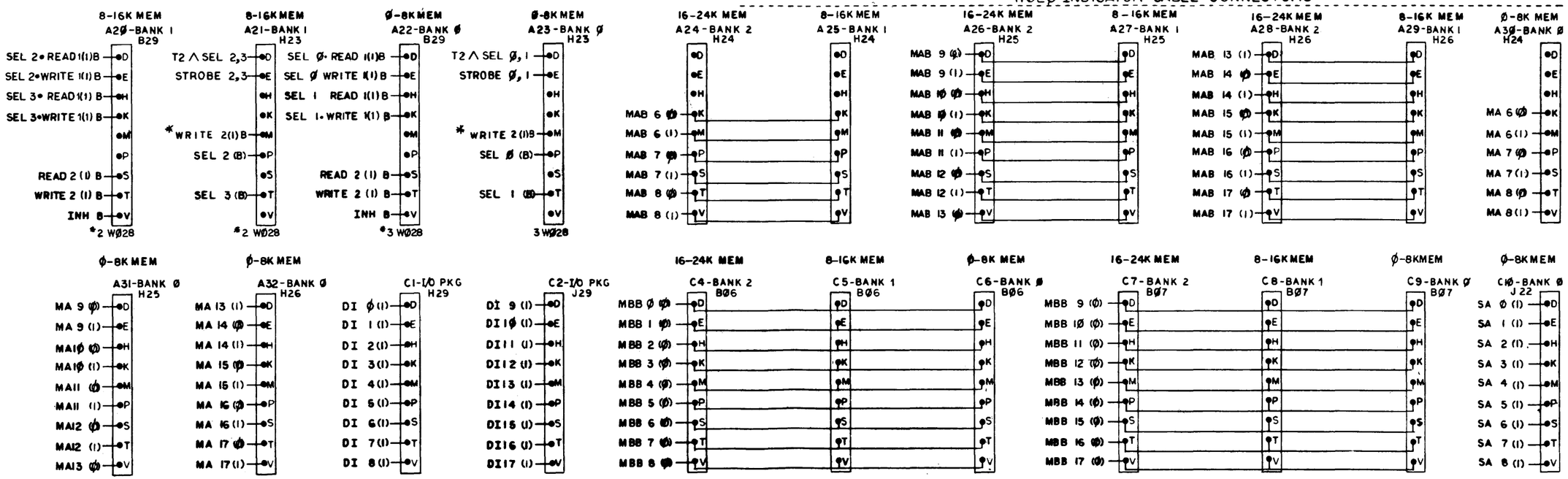
NOTE:
ADD 3K TO -15V ON ONE AND ZERO OUTPUT OF B21Ø'S BITS LINK 1,2,17.

WØ21 SIGNAL CABLE CONNECTORS
UNLESS OTHERWISE SPECIFIED





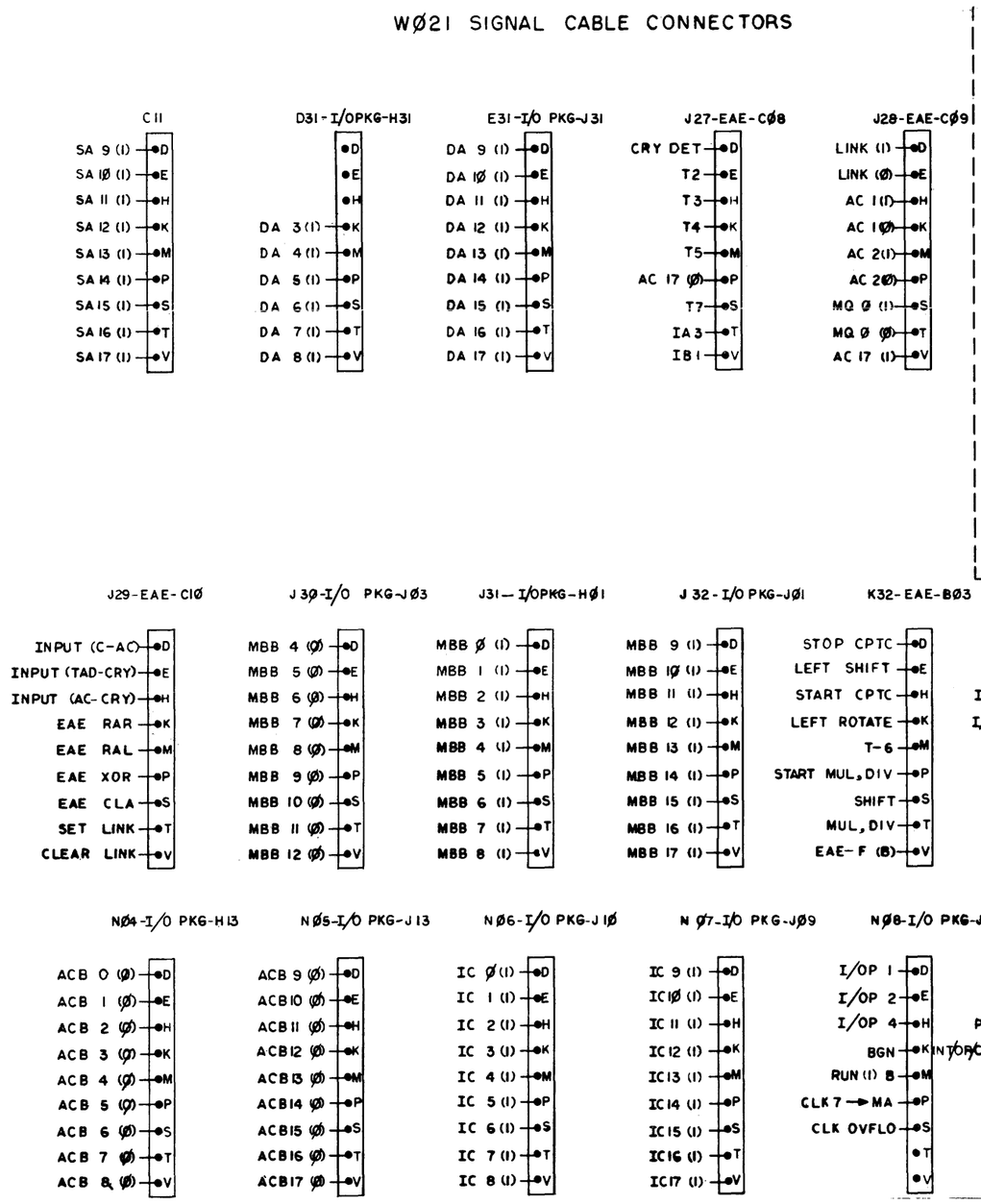
WØ2Ø INDICATOR CABLE CONNECTORS



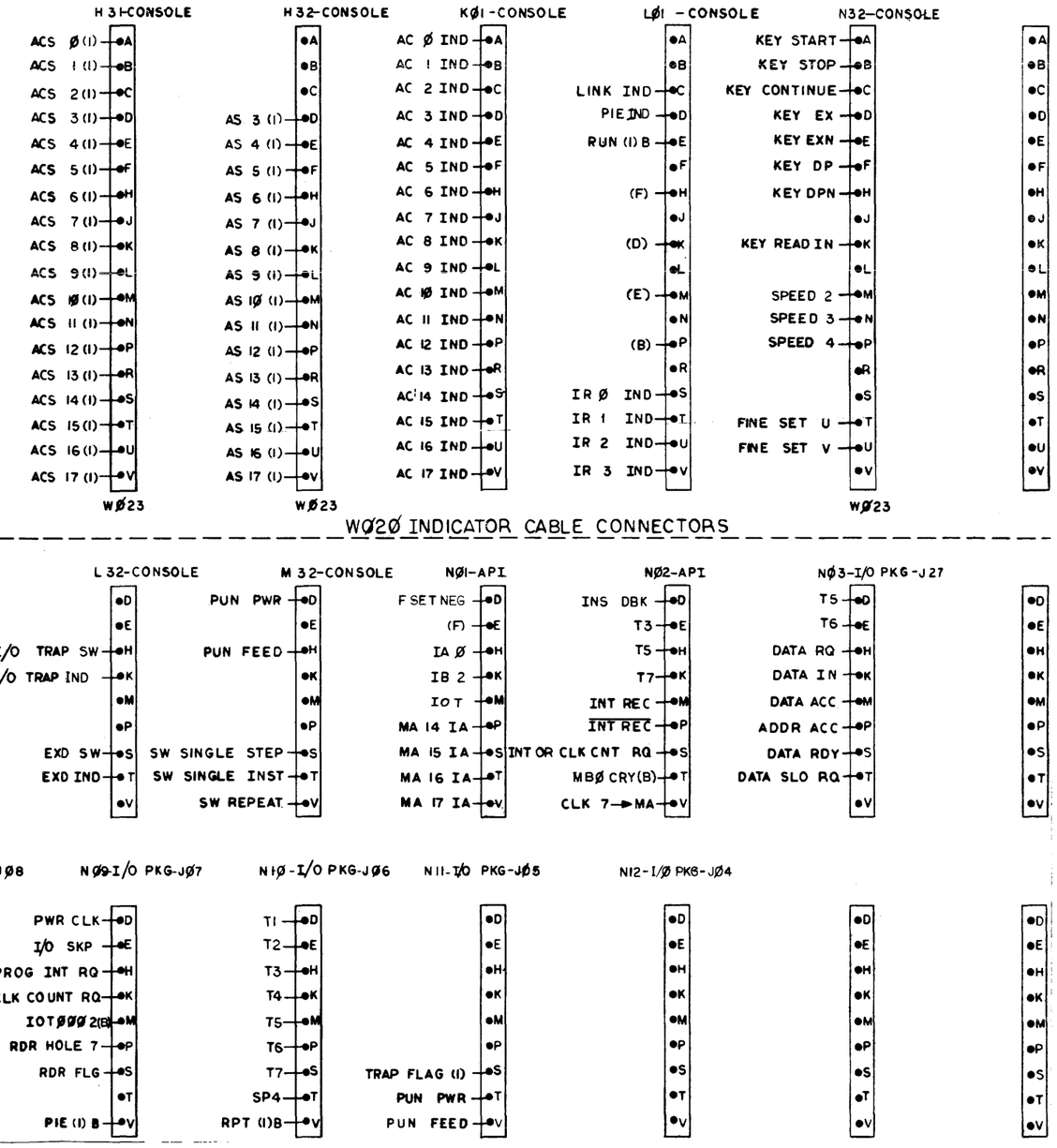
* 1. USED ONLY FOR MEMORY SIMULATOR
# 2. SEE D-7A-Ø-13 FOR WØ28 DETAILS.
#3. SEE D-7A-Ø-9 FOR WØ28 DETAILS.

Central Processor Cables Out/In (Sheet 1) CL-D-KA77A-0-20

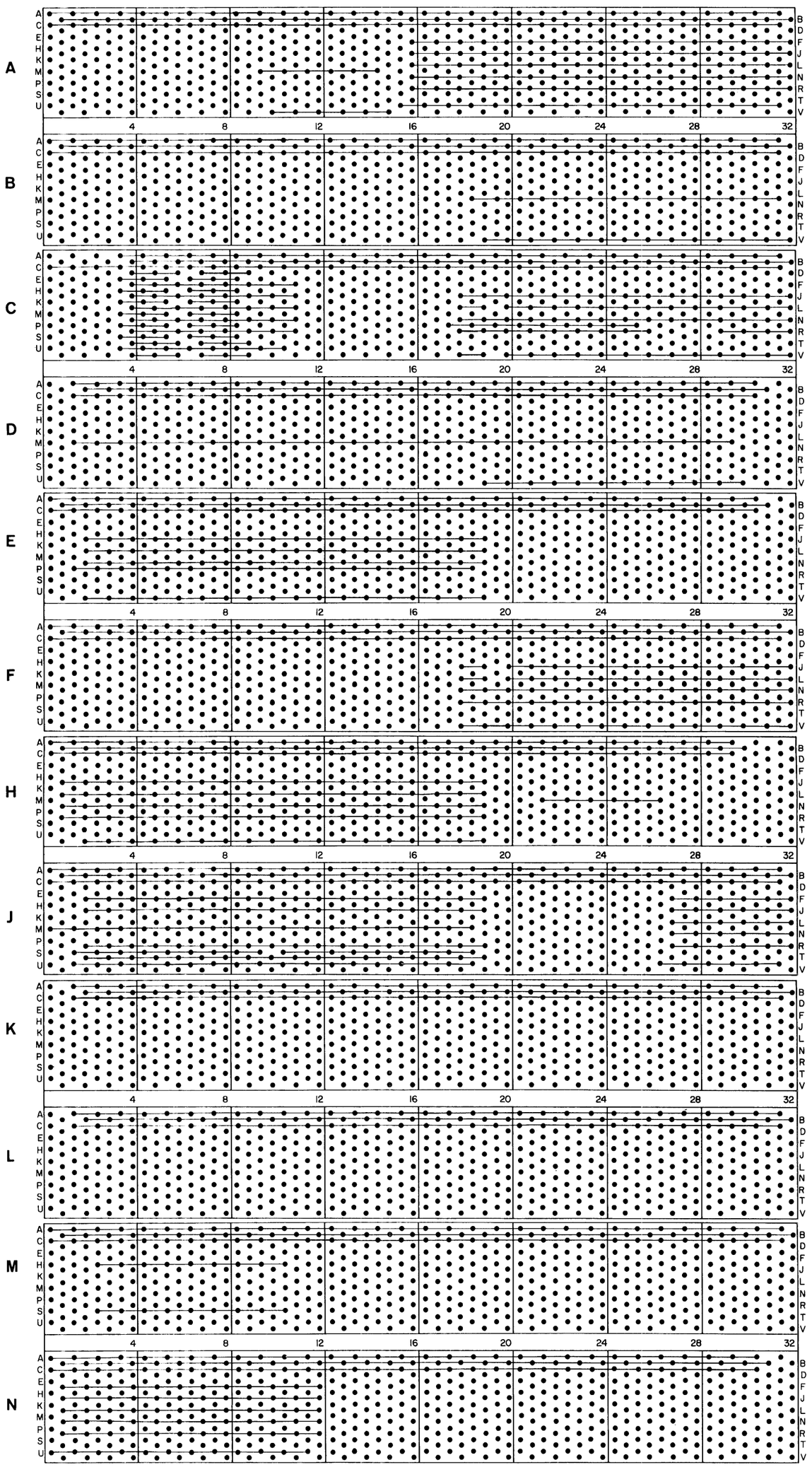
WØ21 SIGNAL CABLE CONNECTORS



WØ20 INDICATOR CABLE CONNECTORS



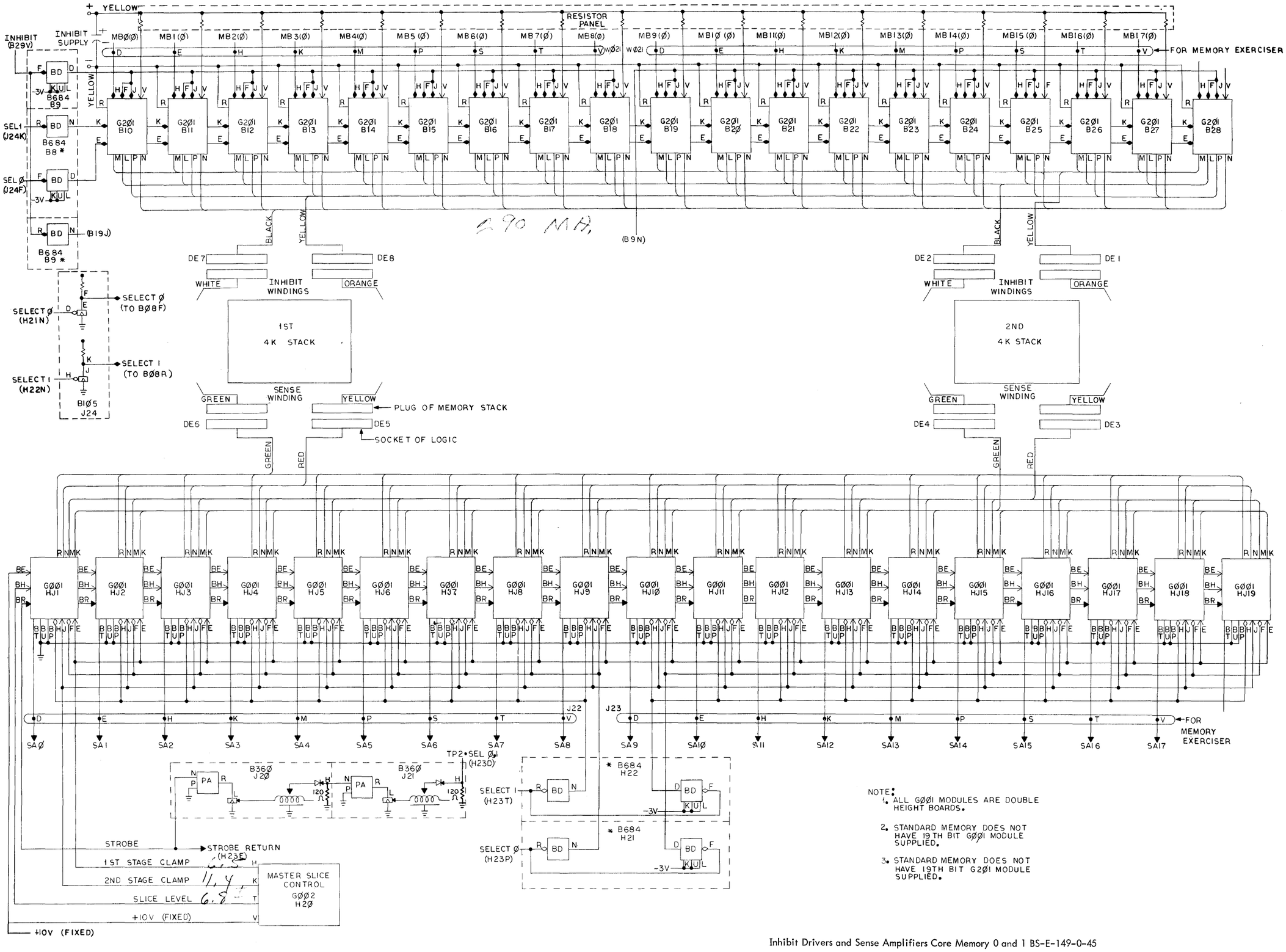
Central Processor Cables Out/In (Sheet 2) CL-D-KA77A-0-20



Bus Bar for Central Processor WD-D-KA77A-0-21

Bus Bar for Central Processor WD-D-KA77A-0-21

REVISIONS			
REV LTR	ECO NO	DATE	ENG
A	5	11-24-65	RPB
B	9	1-7-66	RPB
C	12	1-25-66	RPB
D	14	2-4-66	RPB
E	18	3-11-66	RPB
F	20	3-15-66	RPB

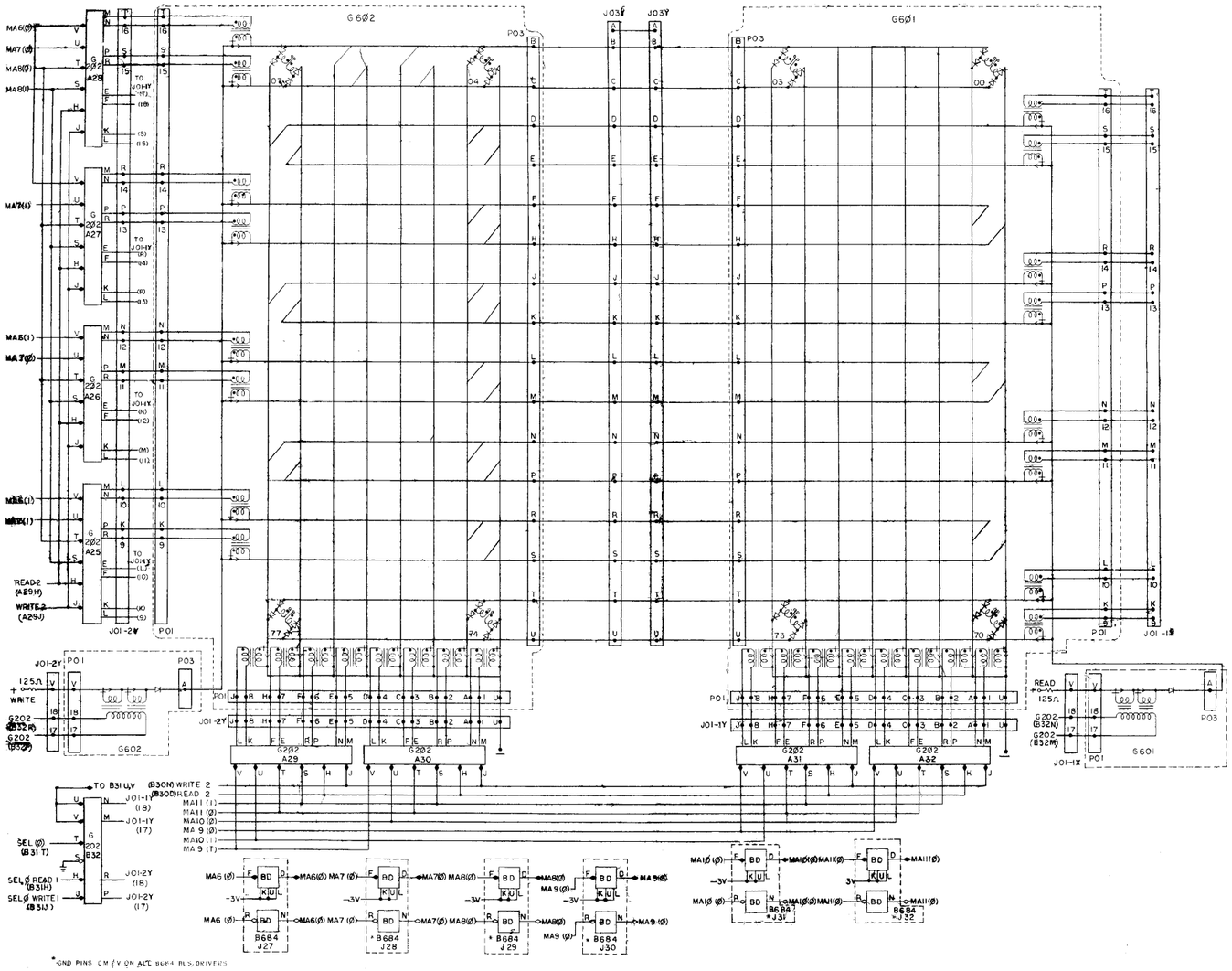


NOTE:
1. ALL GØØ1 MODULES ARE DOUBLE HEIGHT BOARDS.
2. STANDARD MEMORY DOES NOT HAVE 19TH BIT GØØ1 MODULE SUPPLIED.
3. STANDARD MEMORY DOES NOT HAVE 19TH BIT G2Ø1 MODULE SUPPLIED.

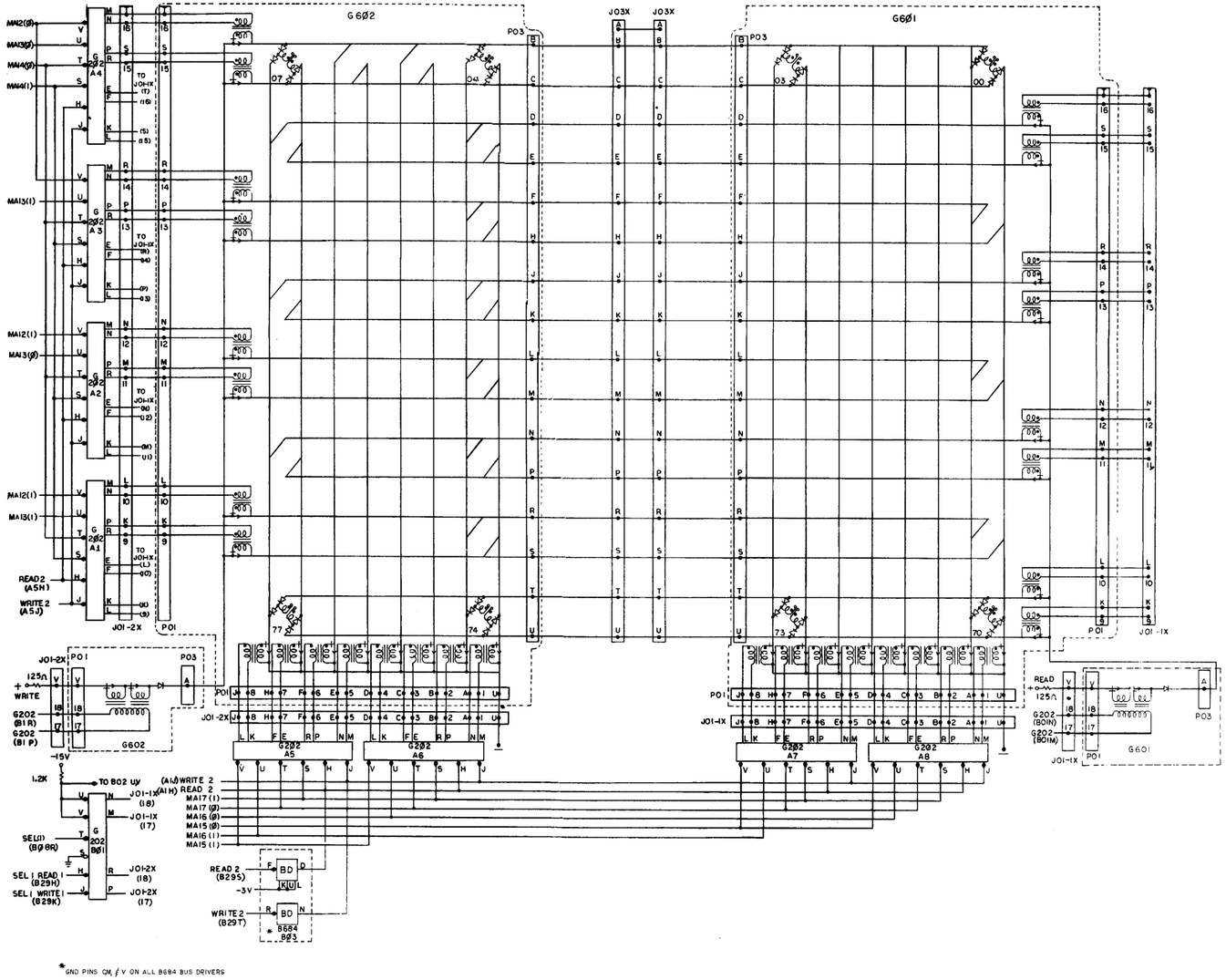
* GND PINS C, M & V ON ALL B684 BUS DRIVERS

Inhibit Drivers and Sense Amplifiers Core Memory 0 and 1 BS-E-149-0-45

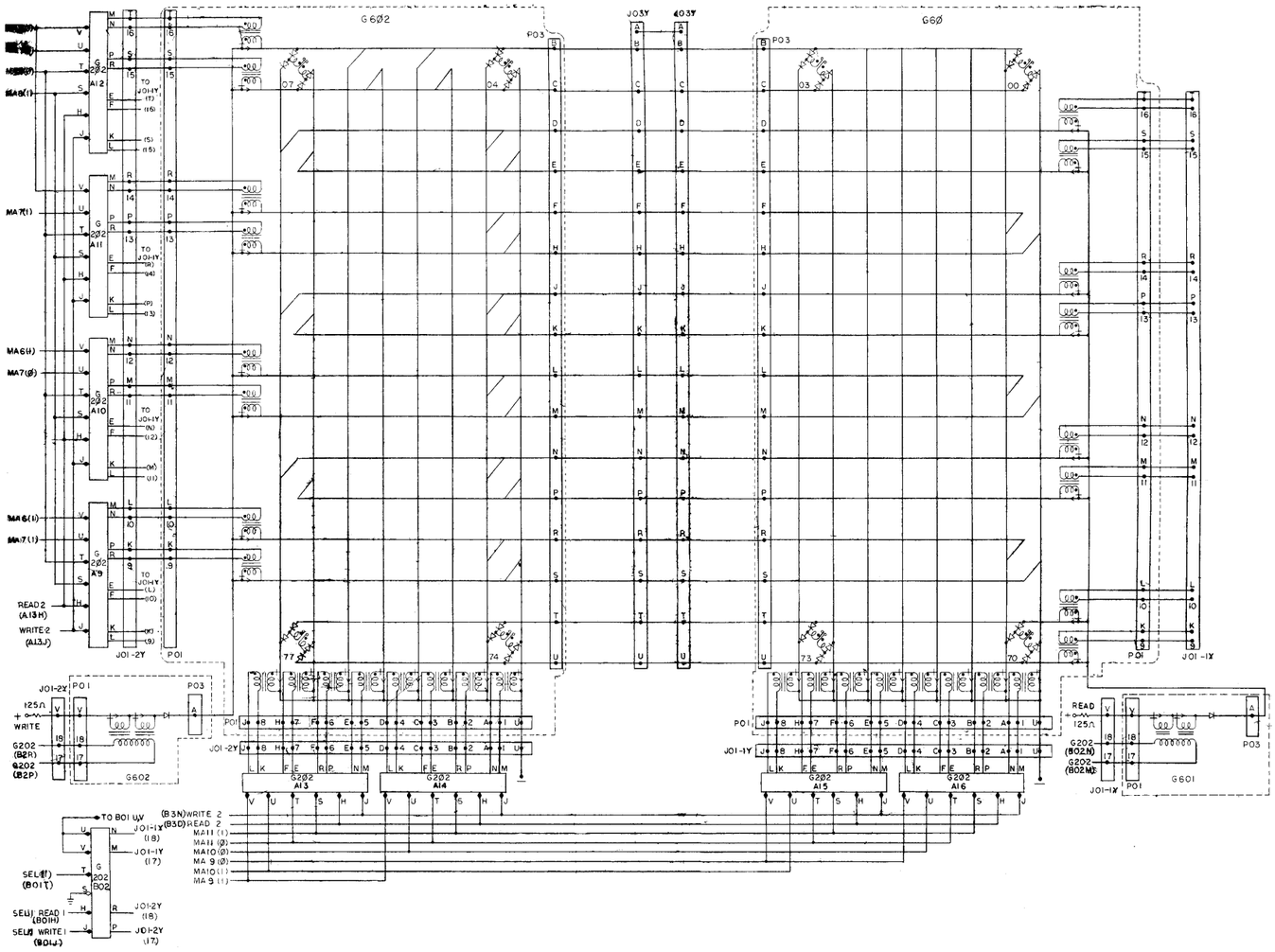
"X" Axis Selection 4K Core Memory BS-E-149-0-46



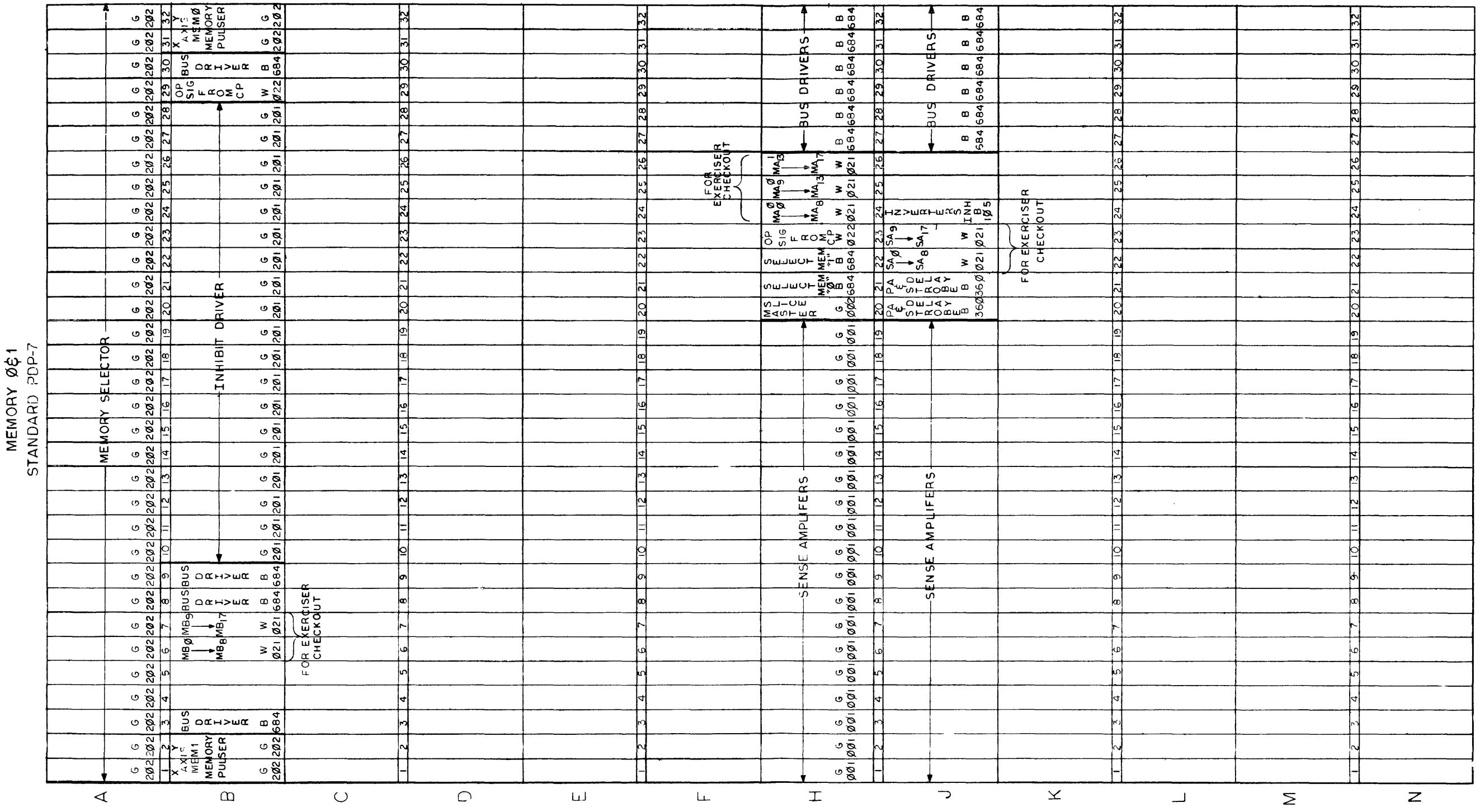
"Y" Axis Selection 4K Core Memory BS-E-149-0-47



"X" Axis Selection of Core Memory BS-E-149-0-48



"Y" Axis Selection of Core Memory BS-E-149-0-49

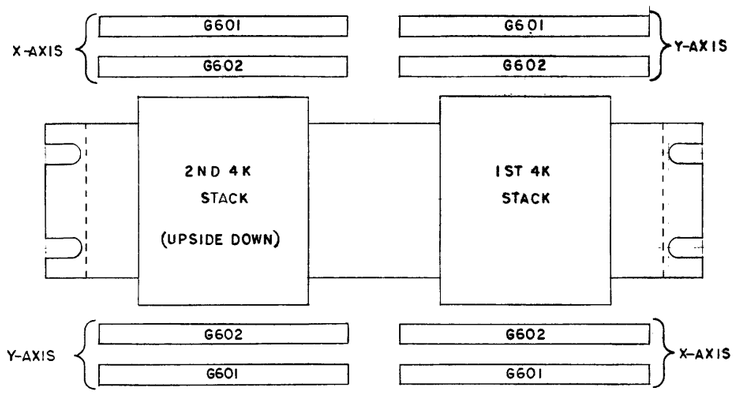


NOTE:
M BUSES A1 THRU A6, AND B1 THRU B3
ARE FOR SECOND 4K MEMORY ONLY

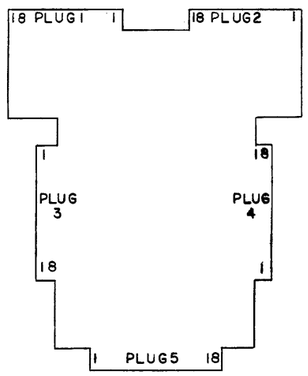
Standard Memory Module Map
ML-D-149-0-50

Standard Memory Module Map ML-D-149-0-50

FRONT PANEL VIEW



G602 OR G601



VIEW FROM COMPONENT SIDE.

NOTE:

LETTERS OF PLUGS ARE ON PRINTED CIRCUIT SIDE OF BOARD.

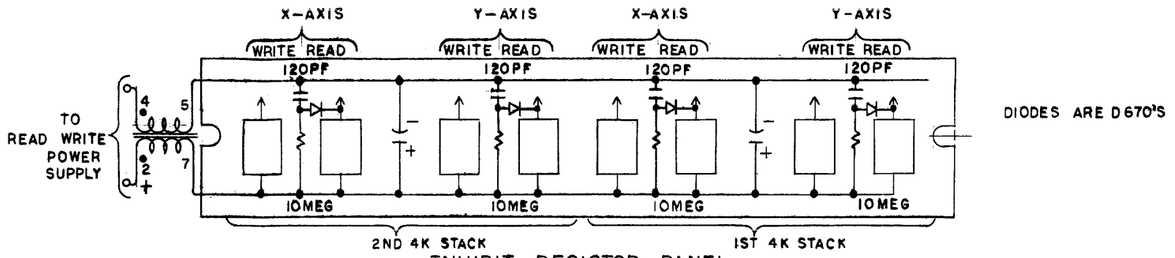
NUMBERS ARE ON COMPONENT SIDE OF BOARD.

EXAMPLE

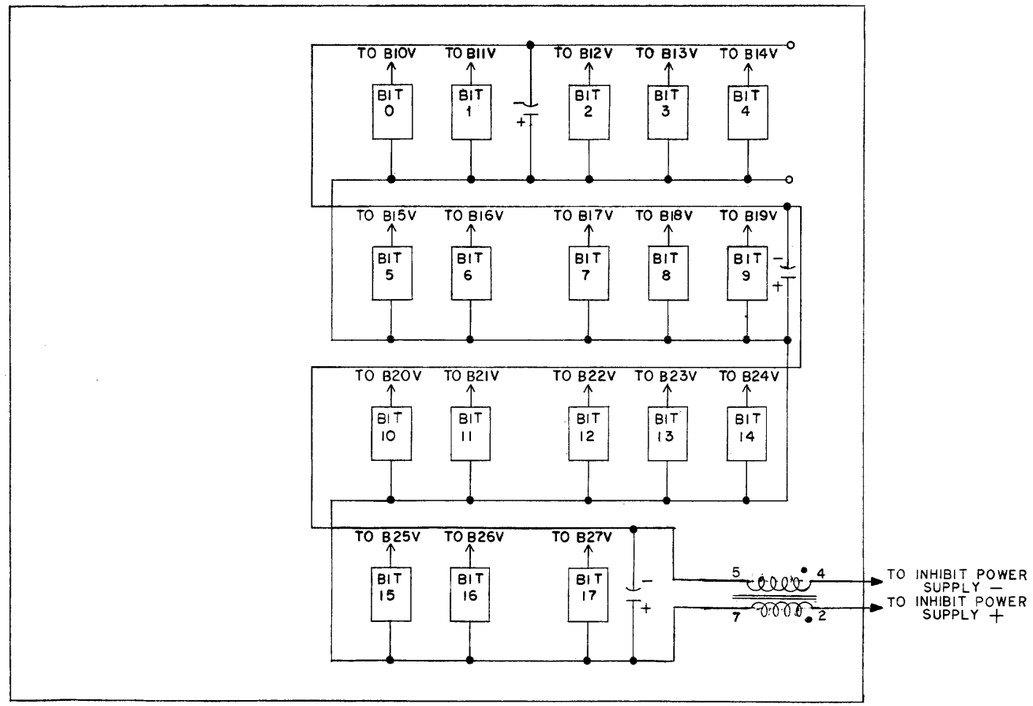
1-C 1-3

FIRST NUMBER (1) REFERS TO PLUG
SECOND LETTER (C) OR NUMBER (3) REFERS TO PINS.

FRONT PANEL VIEW OF READ WRITE RESISTORS



INHIBIT RESISTOR PANEL



NOTE:

1. CAPACITORS ARE 1 MFD, 150V.
2. RESISTORS ARE 125 OHMS ± 1%, 25 WATTS NON-INDUCTIVE.

Resistor Panels WD-D-149-0-51

TOP

CONN	1	2		6	7
PIN	SENSE	SENSE		INH RET	INH DRV
A	0	0′		0	0
B	1	1′		1	1
C	2	2′		2	2
D	3	3′		3	3
E	4	4′		4	4
F	5	5′		5	5
H	6	6′		6	6
J	7	7′		7	7
K	8	8′		8	8
L	9	9′		9	9
M	10	10′		10	10
N	11	11′		11	11
P	12	12′		12	12
R	13	13′		13	13
S	14	14′		14	14
T	15	15′		15	15
U	16	16′		16	16
V	17	17′		17	17
W	* 18	* 18′		* 18	* 18
X					
Y					
Z					
WIRE COLOR	WHITE **	RED **	CONNECTORS MOUNTED ON CASTING ASSEMBLY	WHITE **	BLACK **

CONNECTOR CONFIGURATION FOR SENSE AND INHIBIT WINDINGS

TOP

GREY BLACK GREY BLACK

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	
DWG NO.	73	53	33	13	72	52	32	12	71	51	31	11	70	50	30	10			J05-1Y
A-149-0-43	63	43	23	03	62	42	22	02	61	41	21	01	60	40	20	00			
	A	B	C	D	E	F	H	J	K	L	M	N	P	R	S	T	U	V	

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	
DWG NO.	77	57	37	17	76	56	36	16	75	55	35	15	74	54	34	14			J05-2Y
A-149-0-44	67	47	27	07	66	46	26	06	65	45	25	05	64	44	24	04			
	A	B	C	D	E	F	H	J	K	L	M	N	P	R	S	T	U	V	

FRONT VIEW OF STACK

SOCKETS ARE MOUNTED ON FRONT MOUNTING PLATE

	V	U	T	S	R	P	N	M	L	K	J	H	F	E	D	C	B	A	
DWG NO.			04	24	44	64	05	25	45	65	06	26	46	66	07	27	47	67	J05-2X
A-149-0-42			14	34	54	74	15	35	55	75	16	36	56	76	17	37	57	77	
	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

	V	U	T	S	R	P	N	M	L	K	J	H	F	E	D	C	B	A	
DWG NO.			00	20	40	60	01	21	41	61	02	22	42	62	03	23	43	63	J05-1X
A-149-0-41			10	30	50	70	11	31	51	71	12	32	52	72	13	33	53	73	
	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

BROWN YELLOW BROWN YELLOW

CONNECTOR CONFIGURATION AND ADDRESS LOCATION OF R/W WINDING, READ DRIVE END

TOP

BLACK GREY BLACK GREY

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	
DWG NO.			10	30	50	70	11	31	51	71	12	32	52	72	13	33	53	73	J02-1Y
A-149-0-39			00	20	40	60	01	21	41	61	02	22	42	62	03	23	43	63	
	A	B	C	D	E	F	H	J	K	L	M	N	P	R	S	T	U	V	

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	
DWG NO.			14	34	54	74	15	35	55	75	16	36	56	76	17	37	57	77	J02-2Y
A-149-0-40			04	24	44	64	05	25	45	65	06	26	46	66	07	27	47	67	
	A	B	C	D	E	F	H	J	K	L	M	N	P	R	S	T	U	V	

BACK VIEW OF STACK

SOCKETS ARE FLOATING * * *

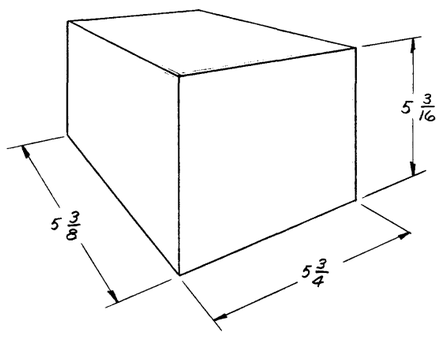
	V	U	T	S	R	P	N	M	L	K	J	H	F	E	D	C	B	A	
DWG NO.	67	47	27	07	66	46	26	06	65	45	25	05	64	44	24	04			J02-2X
A-149-0-38	77	57	37	17	76	56	36	16	75	55	35	15	74	54	34	14			
	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

	V	U	T	S	R	P	N	M	L	K	J	H	F	E	D	C	B	A	
DWG NO.	63	43	23	03	62	42	22	02	61	41	21	01	60	40	20	00			J02-1X
A-149-0-37	73	53	33	13	72	52	32	12	71	51	31	11	70	50	30	10			
	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

YELLOW BROWN YELLOW BROWN

CONNECTOR CONFIGURATION AND ADDRESS LOCATION OF R/W WINDING, READ RETURN END

ALUMINUM HOUSING FOR STACK



HOUSING CONSISTS OF HALVES BOLTED TOGETHER FOR EASY DISASSEMBLY

NOTES:

* FOR STACK WITH 19 PLANES, THESE PINS ARE USED FOR 19TH SENSE AND INHIBIT WINDINGS.

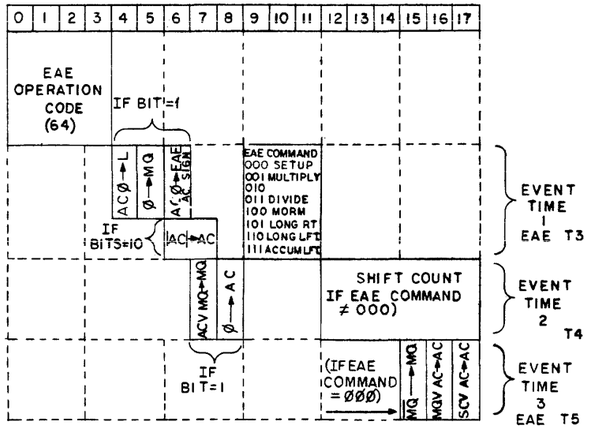
** EACH PAIR OF SENSE WINDINGS WILL BE TWISTED. EACH PAIR OF INHIBIT WINDINGS WILL BE TWISTED.

*** LENGTH OF CABLES FROM SOCKETS TO REAR MOUNTING PLATES IS 10 INCHES.

Memory Stack Connector Configuration CL-D-149-0-52

Memory Stack Connector Configuration CL-D-149-0-52

Figures on pages 6-85 through 6-93 deleted (obsolete)



EAE INSTRUCTION BIT ASSIGNMENT

T1		
T2	STROBE EAE; 1→EAE-F	Ø→EAE-F MUL•MQ 17(1): 1→STOP SHIFT, 1→ADD DIV: 1→SUB, Ø→STOP SHIFT
T3	Ø→STOP SHIFT, Ø→ADD, Ø→SUB MB4(1): ACØ→L SET/CLR→LINK MB5(1): Ø→MQ MB6(1): ACØ→EAE AC SIGN MB6(1) • MB7(Ø) • ACØ(1): $\overline{AC}$→AC OTHER: MB12-17→SC12-17	MUL V DIV: START MUL, DIV, Ø→LINK
T4	MB7(1): AC1→MQ MB8(1): Ø→AC	
T5	SETUP • MB15(1): {1→MQZ, Ø→MQZ} ($\overline{MQ}$→MQ) SETUP•MB16(1): MQ1→AC SETUP • MB17(1): SC1→AC MB9(Ø) • MB10(Ø) • MB11(1): 1→MUL MB9(Ø) • MB10(1): 1→DIV, 1→DIV FIRST SC 12-17=77: 1→FULL MB8(Ø)•NORMALIZE•ACØ⊻AC1: 1→FULL MUL, DIV: INHIBIT BK RQ CN CP EAE AC SIGN⊻LINK→EAE SIGN	
T6	MB9(1): START SHIFT	
T7	SETUP: CLR (MUL V DIV)•EAE AC SIGN (1): $\overline{MQ}$→MQ 1→NORM	

DELAY ADJUSTMENT

INITIAL: SET ALL DELAYS TO MAXIMUM EXCEPT:

1. D3Ø (D-177-Ø-5 D3)
   5Ø NS INPUT (D3ØH) TO OUTPUT (D3ØL)
2. D31 (D-177-Ø-5 C2)
   ADJUST FOR MINIMUM
3. A27 (D-177-Ø-6 D5)
   ADJUST FOR MINIMUM

FINAL: ADJUST DELAYS AS SHOWN ON INDIVIDUAL PRINTS. THE ORDER OF ADJUSTMENT IS INDICATED THERE.

WIRING NOTE:

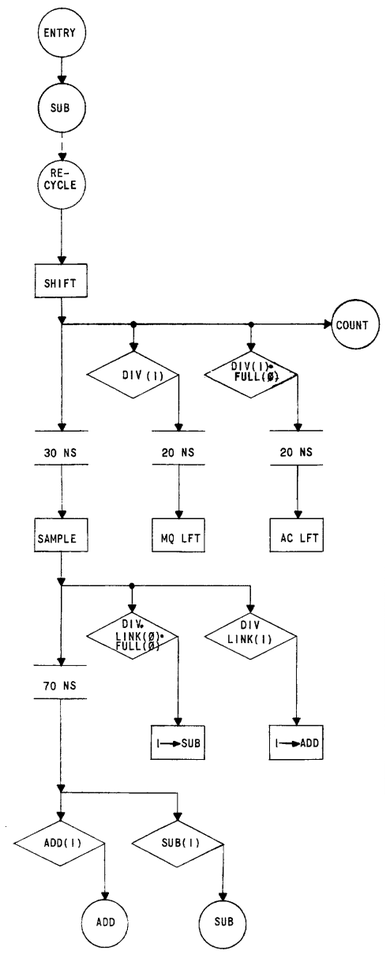
WHEN EAE IS INSTALLED, WIRE:

1. GROUNDS FROM LOWEST PIN IN EAE TO DEVICE SELECTOR HIGHEST PINS
2. BGN: EAE (D2ØL) TO DS(B31V)
3. 1→MQ EAE (A23N) TO EAE (A12T)

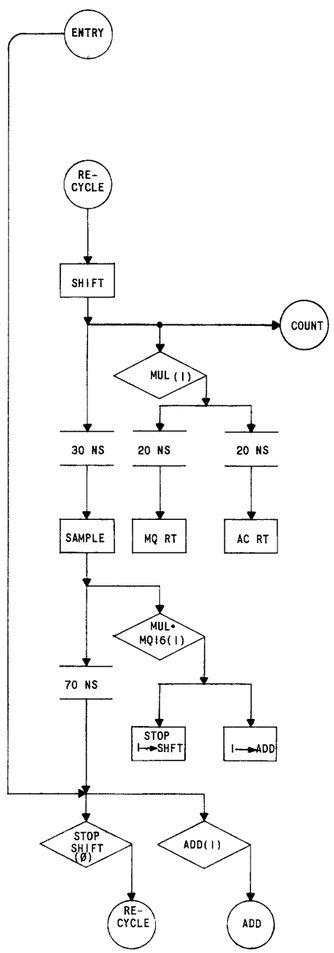
EAE Flow Diagram (Sheet 1) FD-D-177-0-2

EAE Flow Diagram (Sheet 1) FD-D-177-0-2

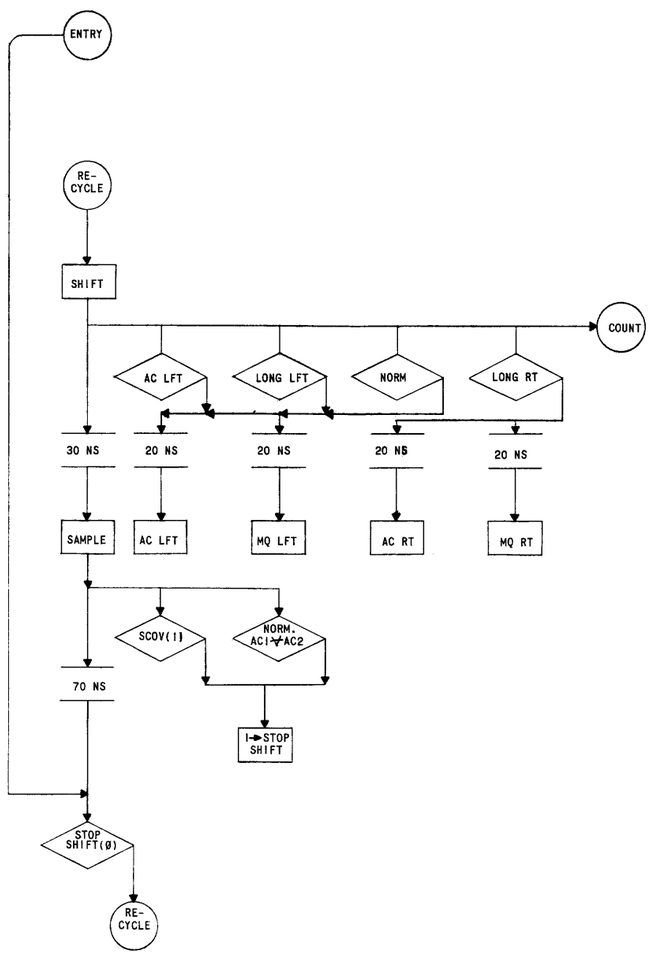
DIVIDE



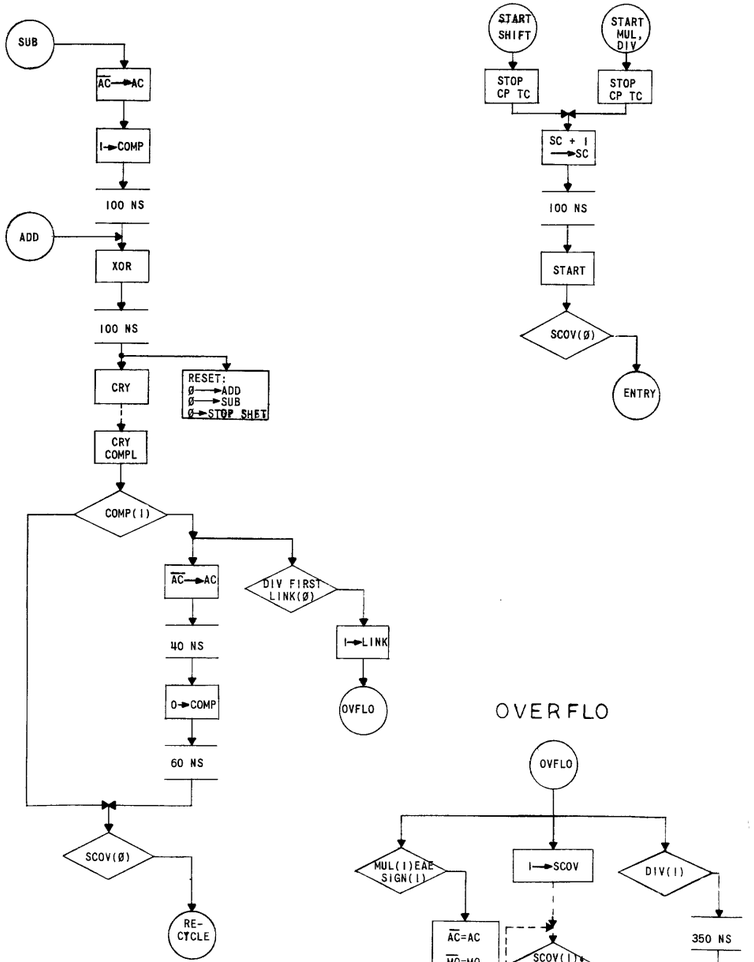
MULTIPLY



SHIFT

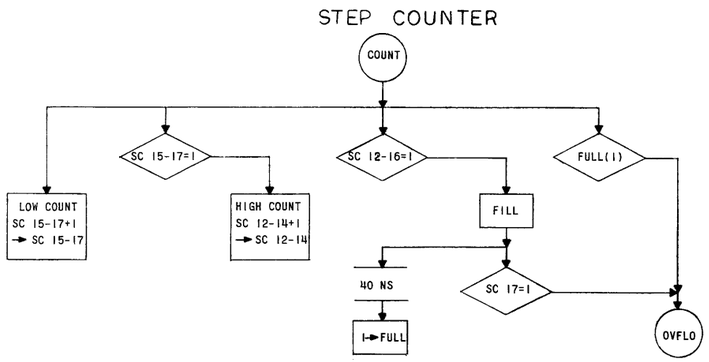


ADDER/SUBTRACTOR



START/END

STEP COUNTER

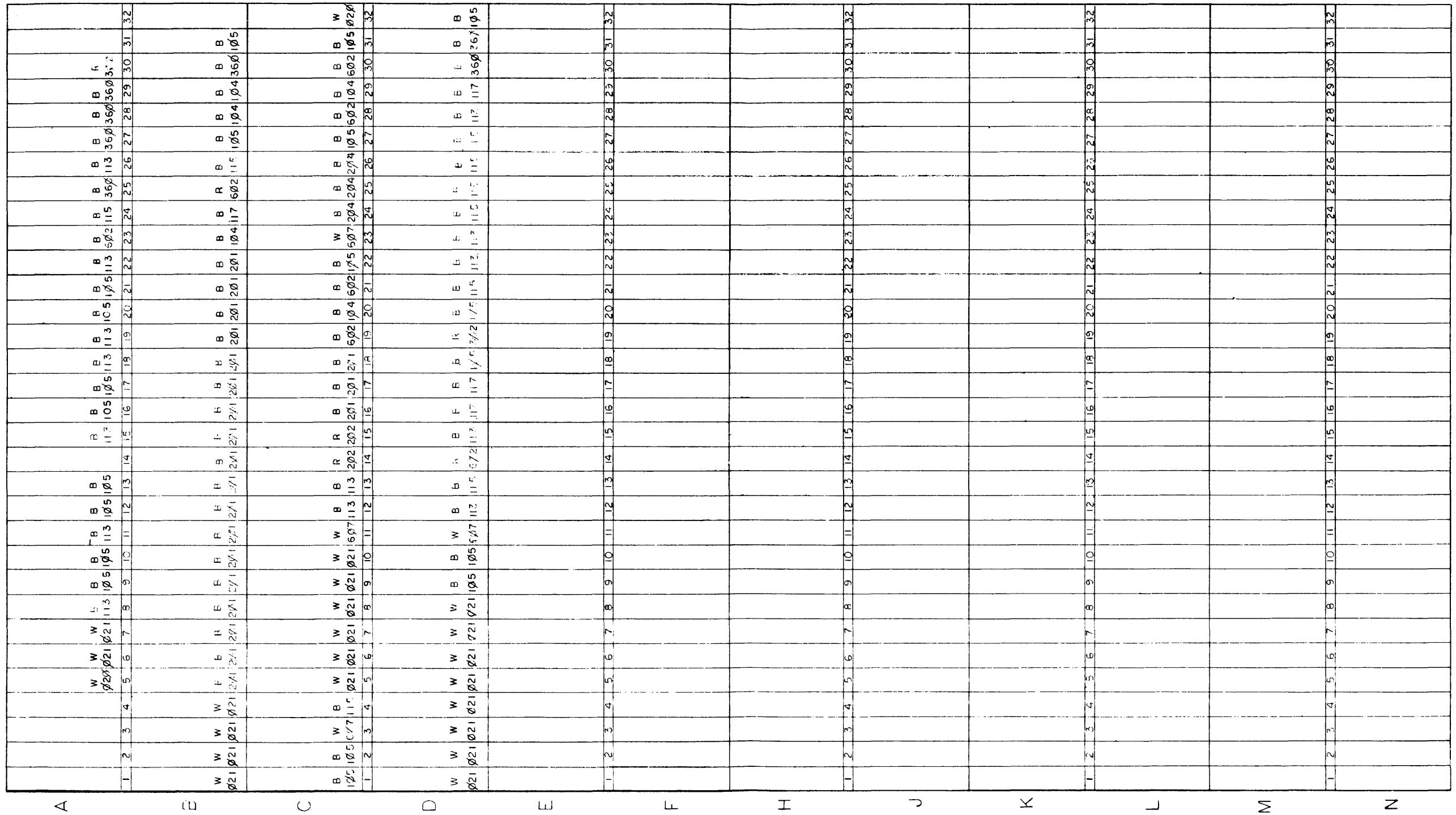


OVERFLO

EAE Flow Diagram (Sheet 2) FD-D-177-0-2

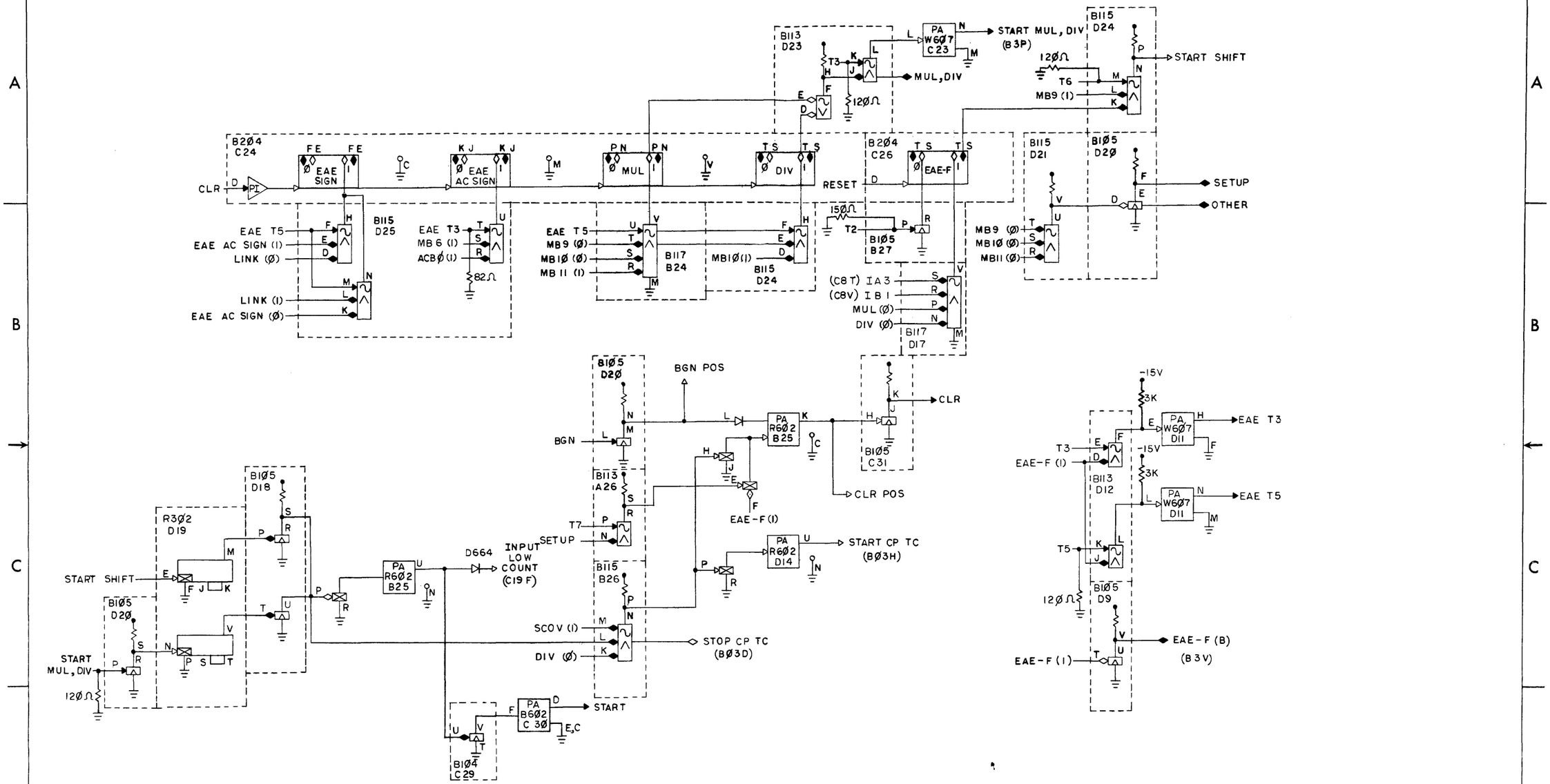
EAE Flow Diagram (Sheet 2) FD-D-177-0-2

EAE MODULE MAP



EAE Module Map
ML-D-177-0-3

EAE Module Map FD-D-177-0-3



NOTE:

1. DELAY ADJUSTMENT

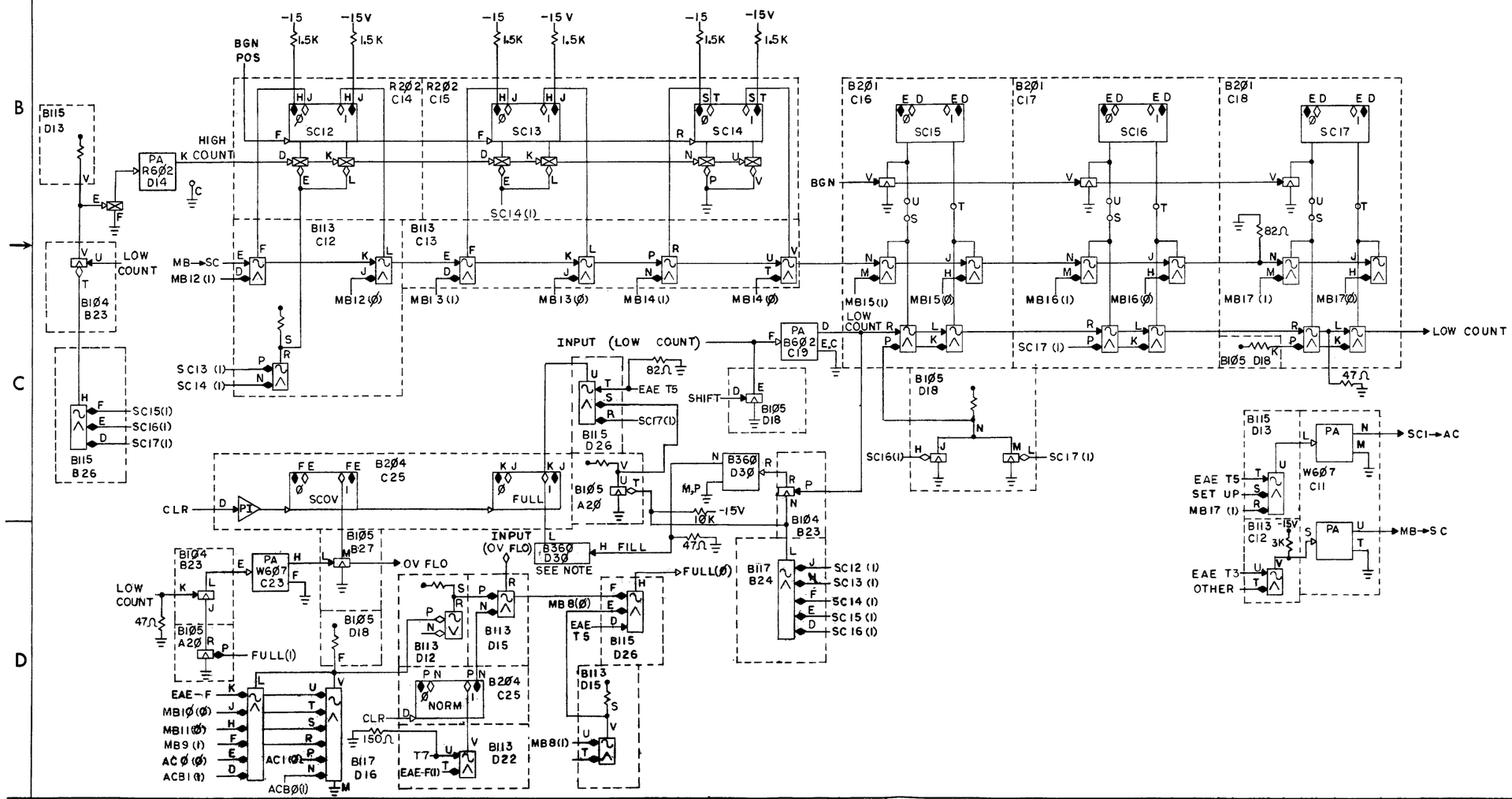
DLY	PROBE 1	PROBE 2	SYNC	CONDITION
8. DI9 UPPER	CP K21J	CP K21K	PROBE 1	LEVEL TO FALL IOONS AFTER PULSE WHILE SHIFTING
9. DI9 LOWER	CP K21J	CP K21K	PROBE 1	AS ABOVE WHILE MULTIPLYING

BKE-2

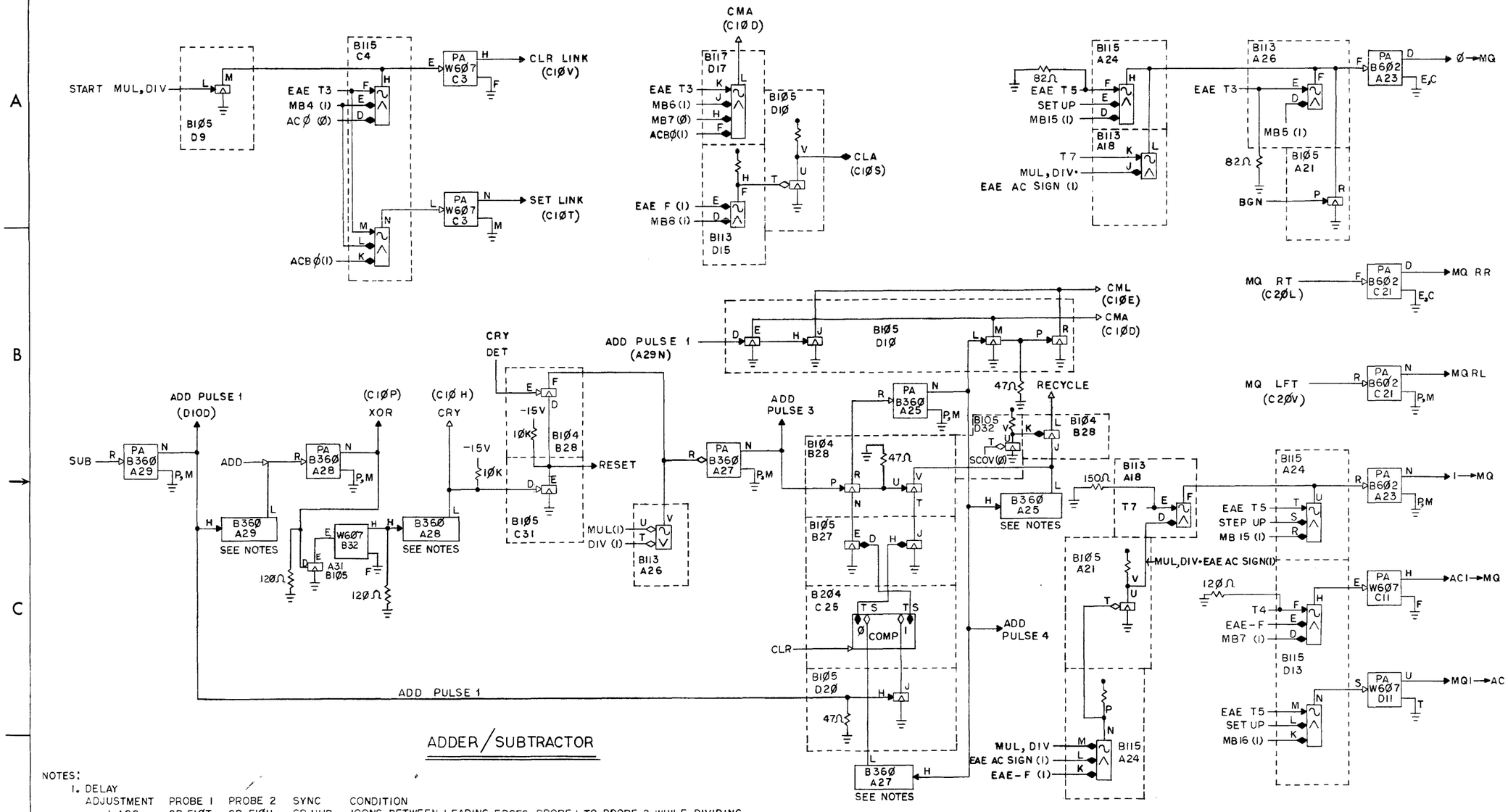
EAE States BS-D-177-0-4

NOTE:
1. DELAY ADJUSTMENT

DLY	PROBE 1	PROBE 2	SYNC	CONDITION
10, D30	EAE D30H	EAE C25J	PROBE 1.	PULSE 50NS BEFORE LEVEL CHANGE BEGINS



EAE Step Counter and Control BS-D-177-0-5

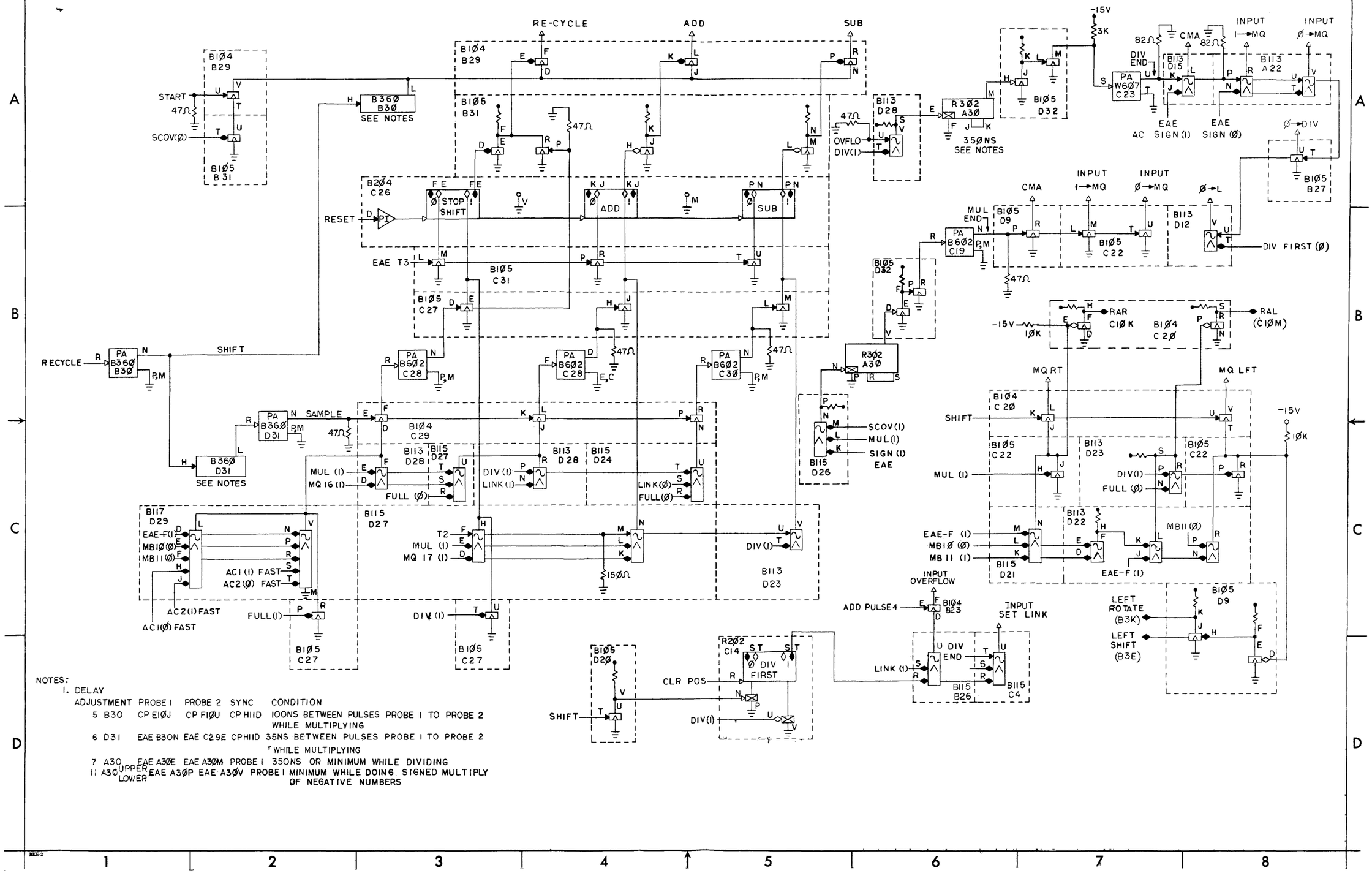


ADDER / SUBTRACTOR

NOTES:

1. DELAY

ADJUSTMENT	PROBE 1	PROBE 2	SYNC	CONDITION
1. A29	CP FIØT	CP FIØU	CP HIID	IOONS BETWEEN LEADING EDGES PROBE 1 TO PROBE 2 WHILE DIVIDING
2. A28	CP FIØU	CP FIØR	CP HIID	IOONS BETWEEN LEADING EDGES PROBE 1 TO PROBE 2 WHILE DIVIDING
3. A25	CP FIØT	CP EIØL	CP HIID	IOONS BETWEEN LEADING EDGES PROBE 1 TO PROBE 2 WHILE DIVIDING
4. A27	EAE A27H	EAE C25S	PROBE 1	IOONS BETWEEN LEADING EDGES PROBE 1 TO PROBE 2 WHILE DIVIDING



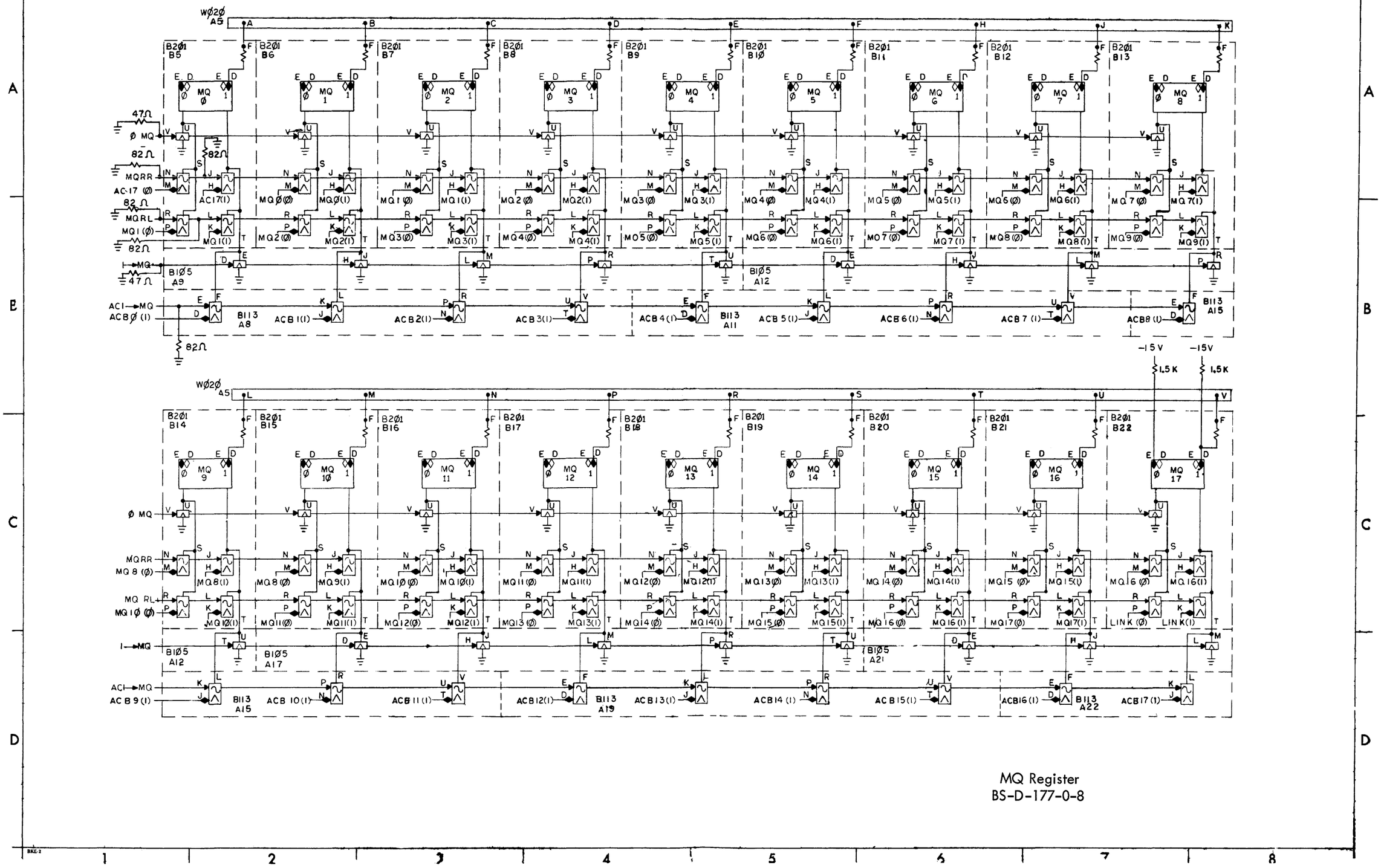
NOTES:

1. DELAY

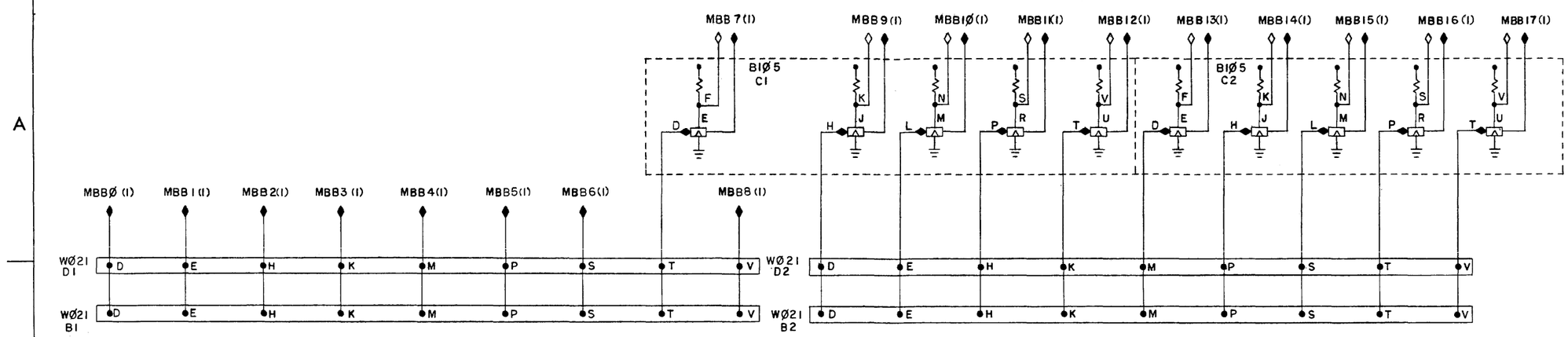
ADJUSTMENT	PROBE 1	PROBE 2	SYNC	CONDITION
5 B30	CP EIØJ	CP FIØU	CP HIID	IOONS BETWEEN PULSES PROBE 1 TO PROBE 2 WHILE MULTIPLYING
6 D31	EAE B3ØN	EAE C29E	CPHIID	35NS BETWEEN PULSES PROBE 1 TO PROBE 2 WHILE MULTIPLYING
7 A30	EAE A3ØE	EAE A3ØM	PROBE 1	350NS OR MINIMUM WHILE DIVIDING
11 A30 UPPER / LOWER	EAE A3ØP	EAE A3ØV	PROBE 1	MINIMUM WHILE DOING SIGNED MULTIPLY OF NEGATIVE NUMBERS

Main Time Chain BS-D-177-0-7

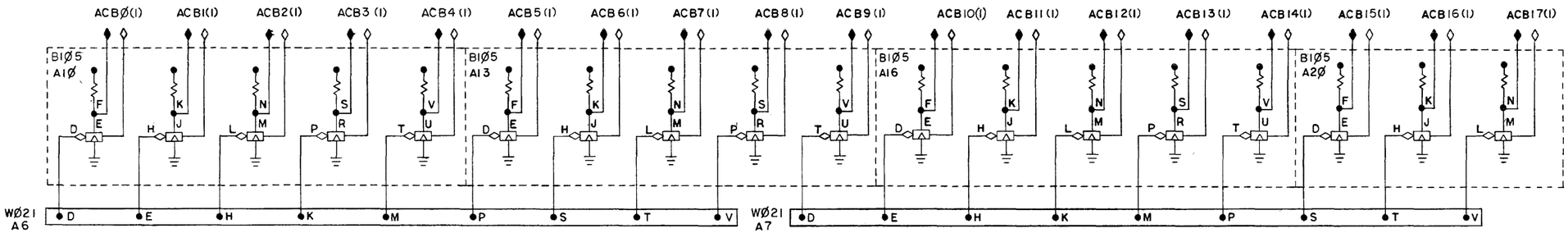
Main Time Chain BS-D-177-0-7



MQ Register
BS-D-177-0-8



* NOTE:
MBBS ARE SERIES TERMINATED
AT DRIVE END.



W021 SIGNAL CABLE CONNECTORS

EAE CABLE TO ID LENGTH 2AØ6 → ILO6

ACBØ (Ø) •D
ACBØ1 (Ø) •E
ACBØ2 (Ø) •H
ACBØ3 (Ø) •K
ACBØ4 (Ø) •M
ACBØ5 (Ø) •P
ACBØ6 (Ø) •S
ACBØ7 (Ø) •T
ACBØ8 (Ø) •V

EAE CABLE TO ID LENGTH 2AØ7 → IMØ6

ACBØ9 (Ø) •D
ACB1Ø (Ø) •E
ACB11 (Ø) •H
ACB12 (Ø) •K
ACB13 (Ø) •M
ACB14 (Ø) •P
ACB15 (Ø) •S
ACB16 (Ø) •T
ACB17 (Ø) •V

MQ INDICATOR CABLE 2AØ5

MQØØ IND •A
MQØ1 IND •B
MQØ2 IND •C
MQØ3 IND •D
MQØ4 IND •E
MQØ5 IND •F
MQØ6 IND •H
MQØ7 IND •J
MQØ8 IND •K
MQØ9 IND •L
MQ1Ø IND •M
MQ11 IND •N
MQ 12 IND •P
MQ 13 IND •R
MQ 14 IND •S
MQ 15 IND •T
MQ 16 IND •U
MQ 17 IND •V

EAE CHECK OUT INDICATOR CABLE 2C32

STOP SHIFT •A
ADD •B
SUB •C
EAE F •D
MUL •E
DIV •F
EAE SIGN •H
EAE AC SIGN •J
FULL •K
SCOV •L
SC 12 •M
SC 13 •N
SC 14 •P
SC 15 •R
SC 16 •S
SC 17 •T
EAE SINGLE STEP SW •U •V

W020 INDICATOR CABLE CONNECTORS

MB BITS FROM CP 2B01 → IF31 *1

MBBØ (I) •D
MBB01 (I) •E
MBB02 (I) •H
MBBØ3 (I) •K
MBBØ4 (I) •M
MBBØ5 (I) •P
MBBØ6 (I) •S
MBBØ7 (I) •T
MBBØ8 (I) •V

MB BITS FROM CP 2B01 → IF32 *

MBB09 (I) •D
MBB1Ø (I) •E
MBB11 (I) •H
MBB12 (I) •K
MBB13 (I) •M
MBB14 (I) •P
MBB15 (I) •S
MBB16 (I) •T
MBB17 (I) •V

CP CONTROL SIGNALS FROM EAE 2B03 → IN32 *2

STOP CP TC •D
LEFT SHIFT •E
START CP TC •H
LEFT ROTATE •K
SC1 - AC •M
START MUL, DIV •P
MQ1 - AC •S
MUL, DIV •T
EAE - F (B) •V

EAE CABLES TO DS 2DØ1 → 2AØ1

MBØ (I) •D
MBØ1 (I) •E
MBØ2 (I) •H
MBØ3 (I) •K
MBØ4 (I) •M
MBØ5 (I) •P
MBØ6 (I) •S
MBØ7 (I) •T
MBØ8 (I) •V

EAE CABLES TO DS 2DØ2 → 2AØ2

MB 9 (I) •D
MB1Ø (I) •E
MB 11 (I) •H
MB 12 (I) •K
MB 13 (I) •M
MB 14 (I) •P
MB 15 (I) •S
MB 16 (I) •T
MB 17 (I) •V

EAE CABLE TO IC (MQ) 2CØ5 → IN1Ø

MQ Ø (I) •D
MQ Ø1 (I) •E
MQ Ø2 (I) •H
MQ Ø3 (I) •K
MQ Ø4 (I) •M
MQ Ø5 (I) •P
MQ Ø6 (I) •S
MQ Ø7 (I) •T
MQ Ø8 (I) •V

EAE CABLE TO IC (MQ) 2CØ6 → IN2Ø

MQ 9 (I) •D
MQ1Ø (I) •E
MQ11 (I) •H
MQ12 (I) •K
MQ13 (I) •M
MQ14 (I) •P
MQ15 (I) •S
MQ16 (I) •T
MQ17 (I) •V

EAE CABLE TO IC STEP COUNTER BITS 2CØ7 → IN28 *4

T6 •D
SHIFT •E
•H
SC 12 (I) •K
SC 13 (I) •M
SC 14 (I) •P
SC 15 (I) •S
SC 16 (I) •T
SC 17 (I) •V

EAE CABLE TO CP 2CØ8 → IF27 (WØ26) *4

CRY DET •D
T2 •E
T3 •H
T4 •K
T5 •M
AC17 (Ø) •P
T7 •S
IA3 •T
IB1 •V

EAE CABLE TO CP 2CØ9 → IF28

•D 82Ω IN SERIES LINK (I)
•E 47Ω IN SERIES LINK (Ø)
•H 47Ω IN SERIES ACI (I)
•K ACI (Ø)
•M AC2 (I)
•P AC2 (Ø)
•S MQØ (I)
•T MQØ (Ø)
•V ACI7 (I)

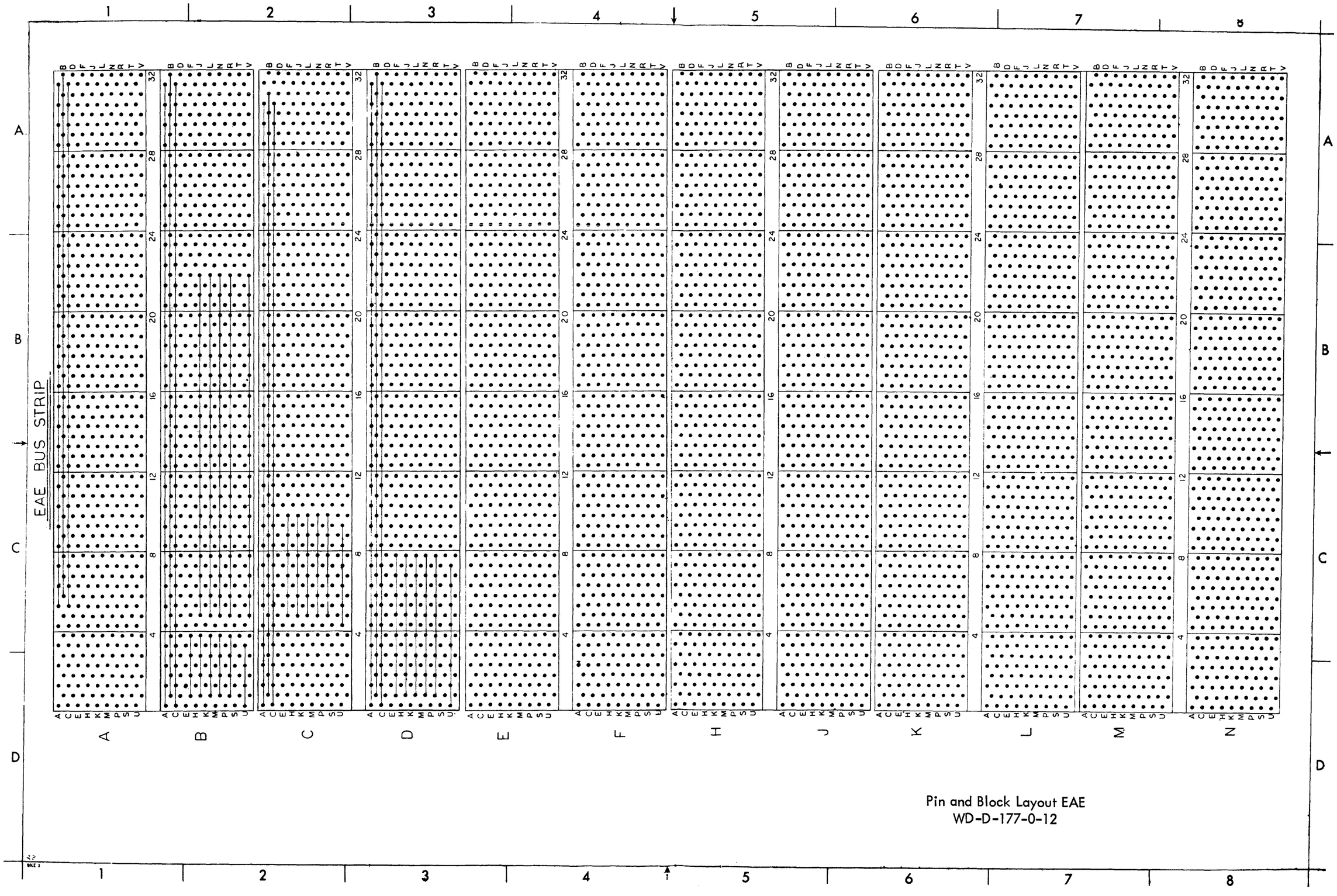
EAE TO CP (WØ28) 2C1Ø → IF29

CMA •D *2 47Ω IN SERIES
CML •E 47Ω IN SERIES
CRY •H 47Ω IN SERIES
RAR •K
RAL •M
XOR •P
CLA •S
SET LINK •T
CLR LINK •V

NOTES:

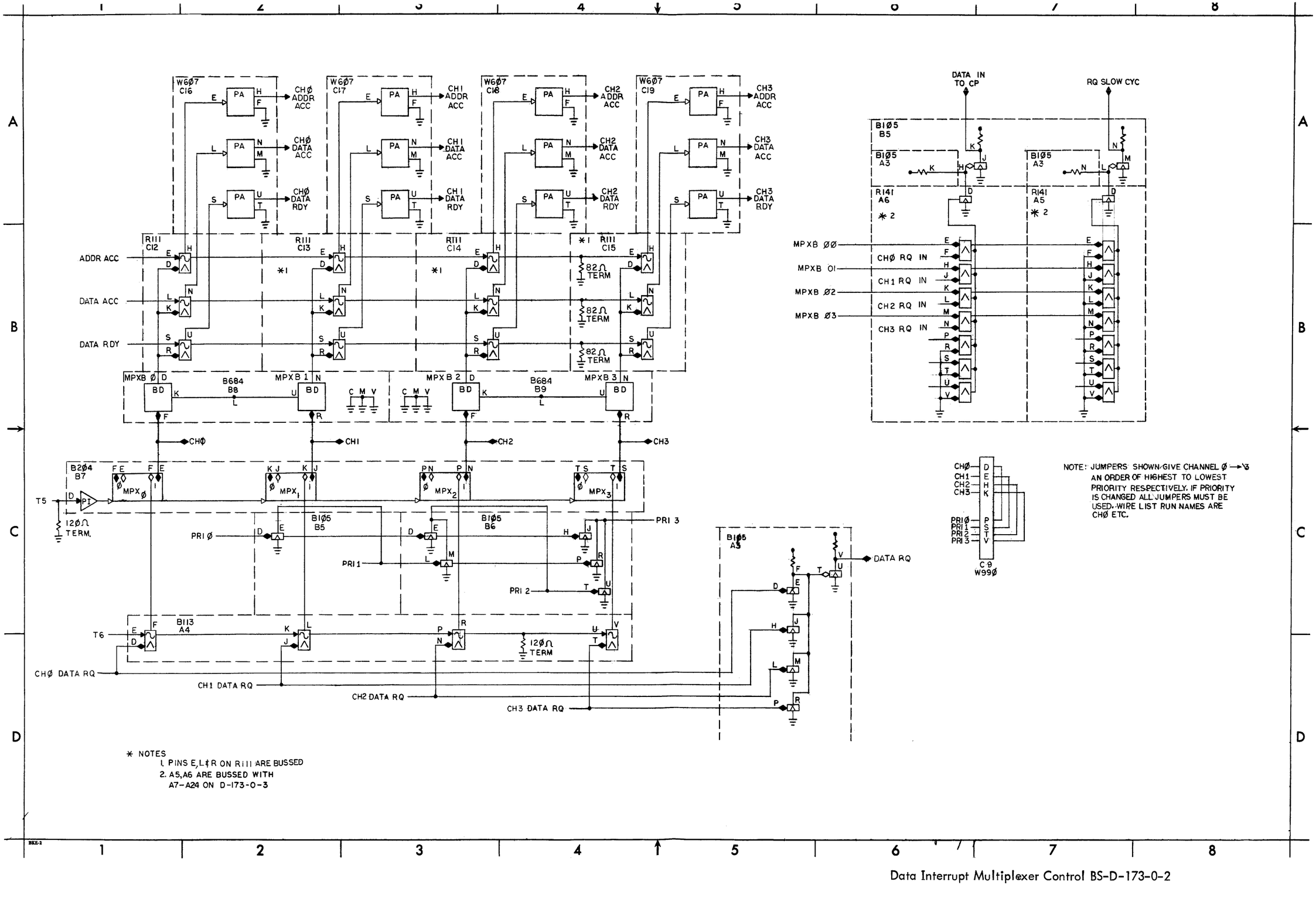
1. CABLE CONNECTOR IS TYPE WØ28 WITH 47 OHM SERIES RESISTORS.
2. REMOVE JUMPER CARD IN CENTRAL PROCESSOR.
3. WHEN EAE IS INSTALLED, THE CABLES GOING TO 2AO1, 2AO2 OF THE DEVICE SELECTOR ARE MOVED TO EAE 2B01, AND 2B02
4. EAE CABLES TO CP W028 CONNECTORS WITH SERIES RESISTORS AS SPECIFIED

EAE Cable Schedules
CL-D-177-0-10

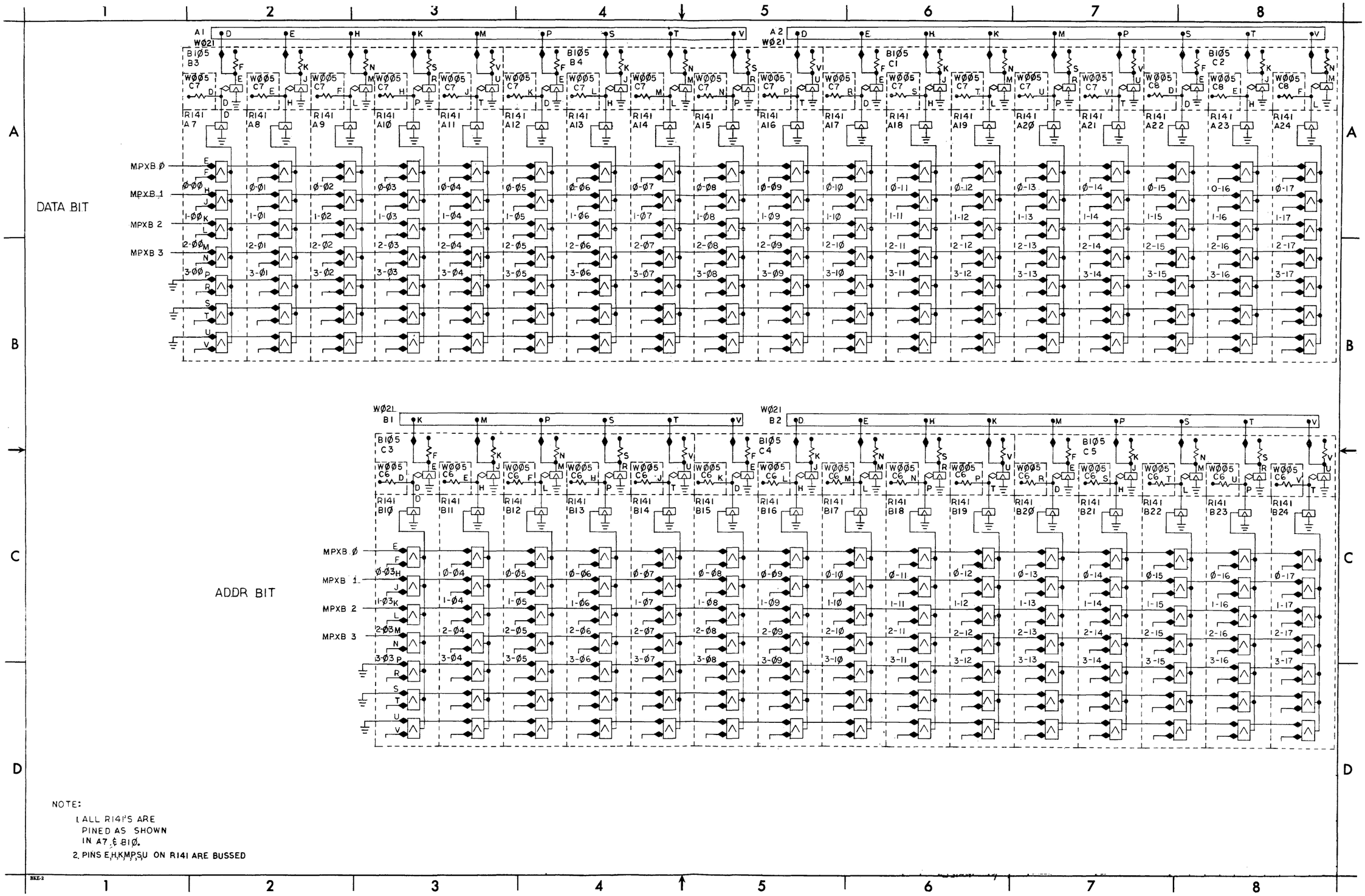


Pin and Block Layout EAE
WD-D-177-0-12

Pin and Block Layout EAE WD-D-177-0-12



Data Interrupt Multiplexer Control BS-D-173-0-2

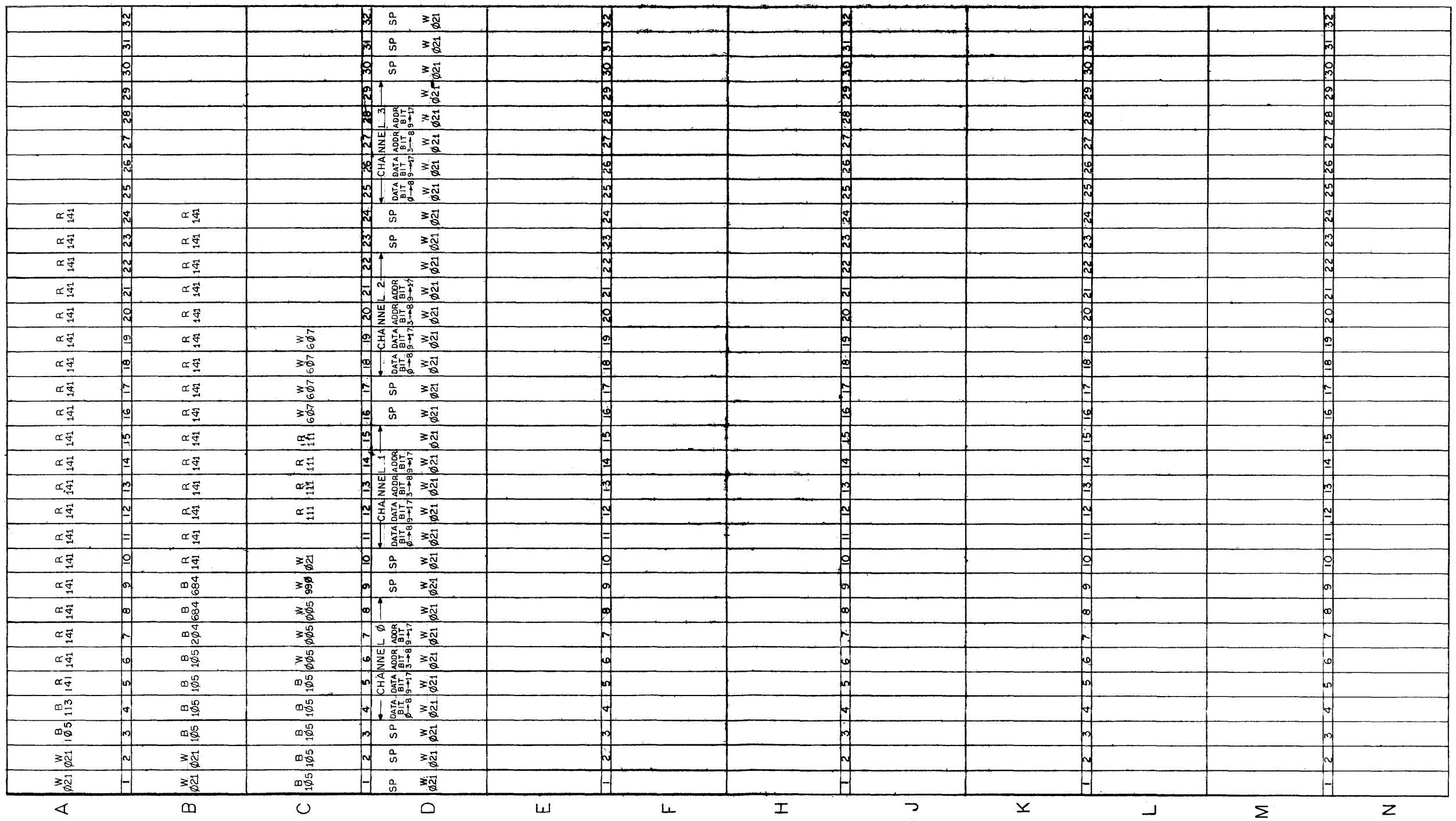


NOTE:

1. ALL R141'S ARE PINED AS SHOWN IN A7 & BIØ.
2. PINS E,H,K,M,P,S,U ON R141 ARE BUSSED

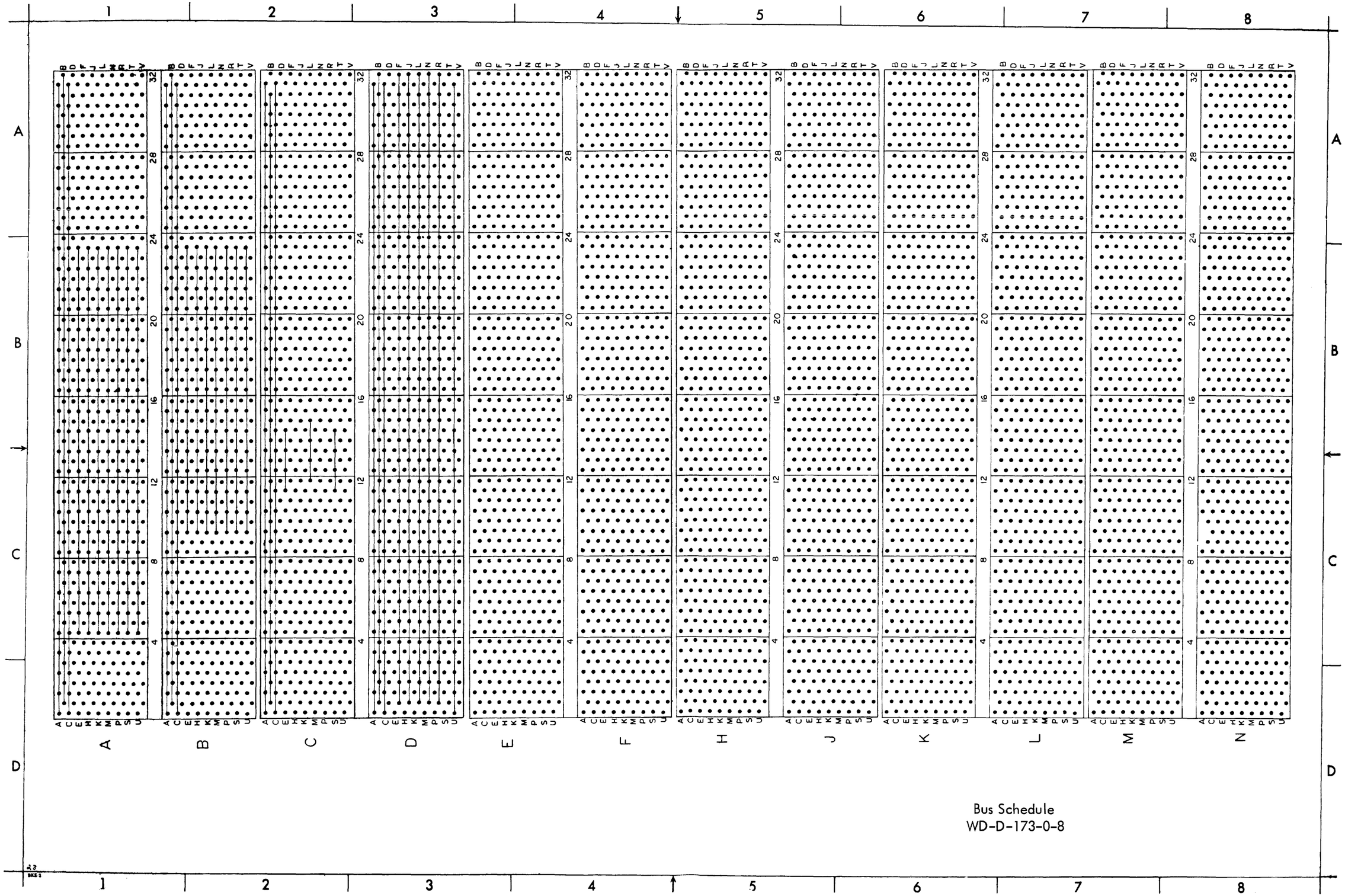
BKE-2

Data Interrupt Multiplexer Data Input/Data Addresses BS-D-173-0-3



Data Interrupt Multiplexer Module Map ML-D-173-0-5

Data Interrupt Multiplexer Module Map ML-D-173-0-5

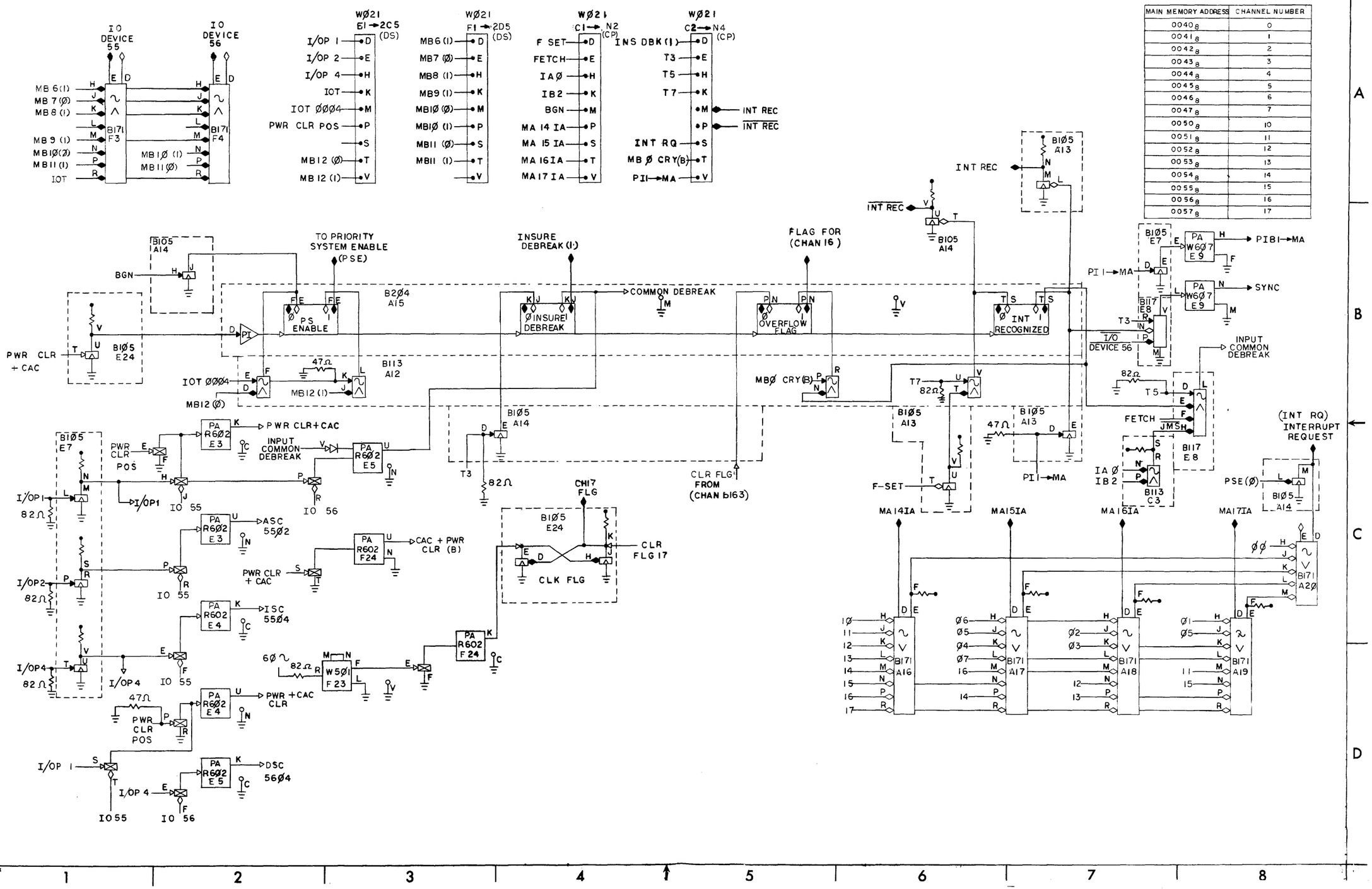


Bus Schedule
WD-D-173-0-8

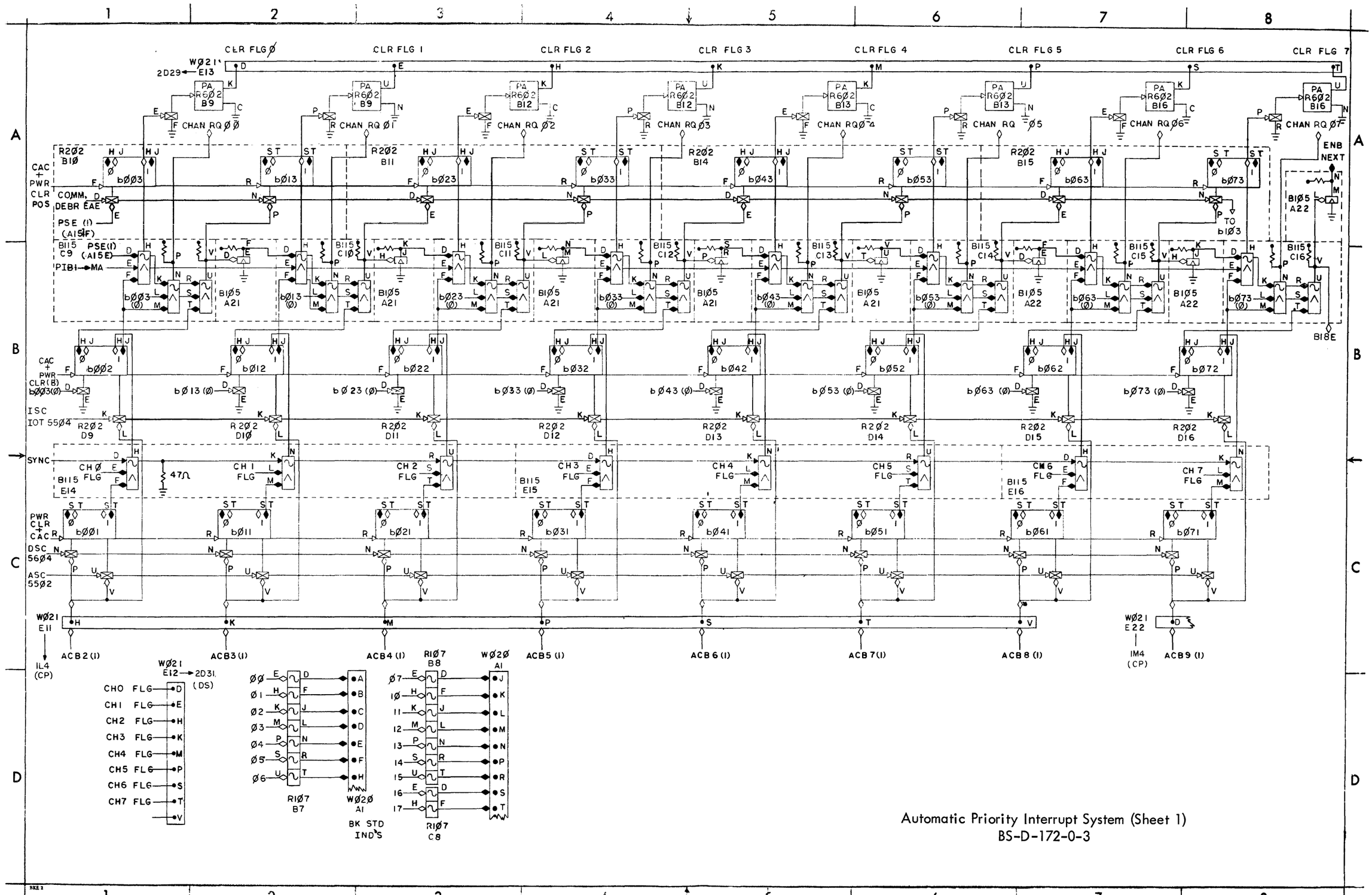
Bus Schedule WD-D-173-0-8

ASSIGNMENT OF MAIN MEMORY LOCATIONS TO CHANNELS

MAIN MEMORY ADDRESS	CHANNEL NUMBER
0040_8	0
0041_8	1
0042_8	2
0043_8	3
0044_8	4
0045_8	5
0046_8	6
0047_8	7
0050_8	10
0051_8	11
0052_8	12
0053_8	13
0054_8	14
0055_8	15
0056_8	16
0057_8	17

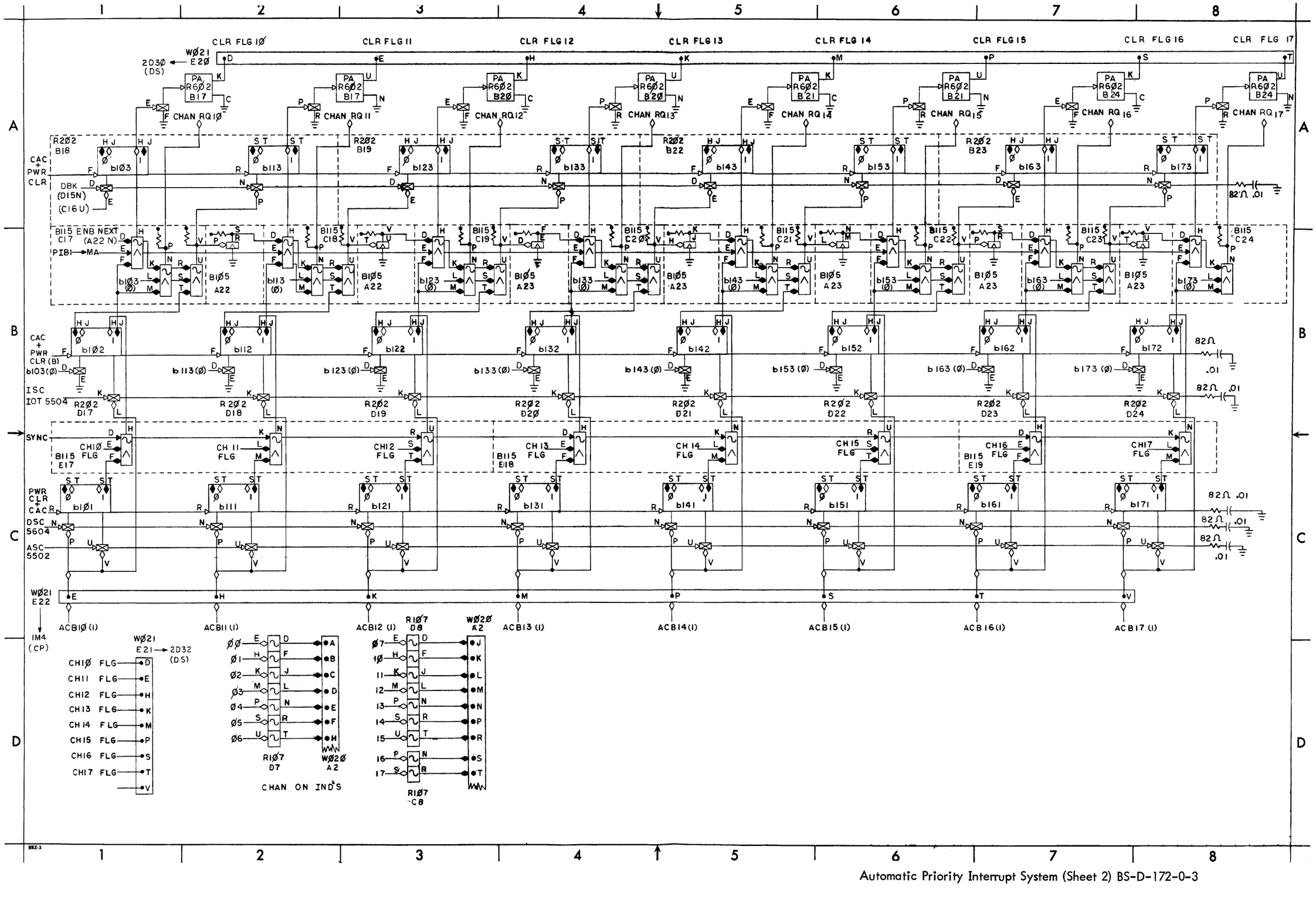


Automatic Priority Interrupt Control BS-D-172-0-2



Automatic Priority Interrupt System (Sheet 1)
BS-D-172-0-3

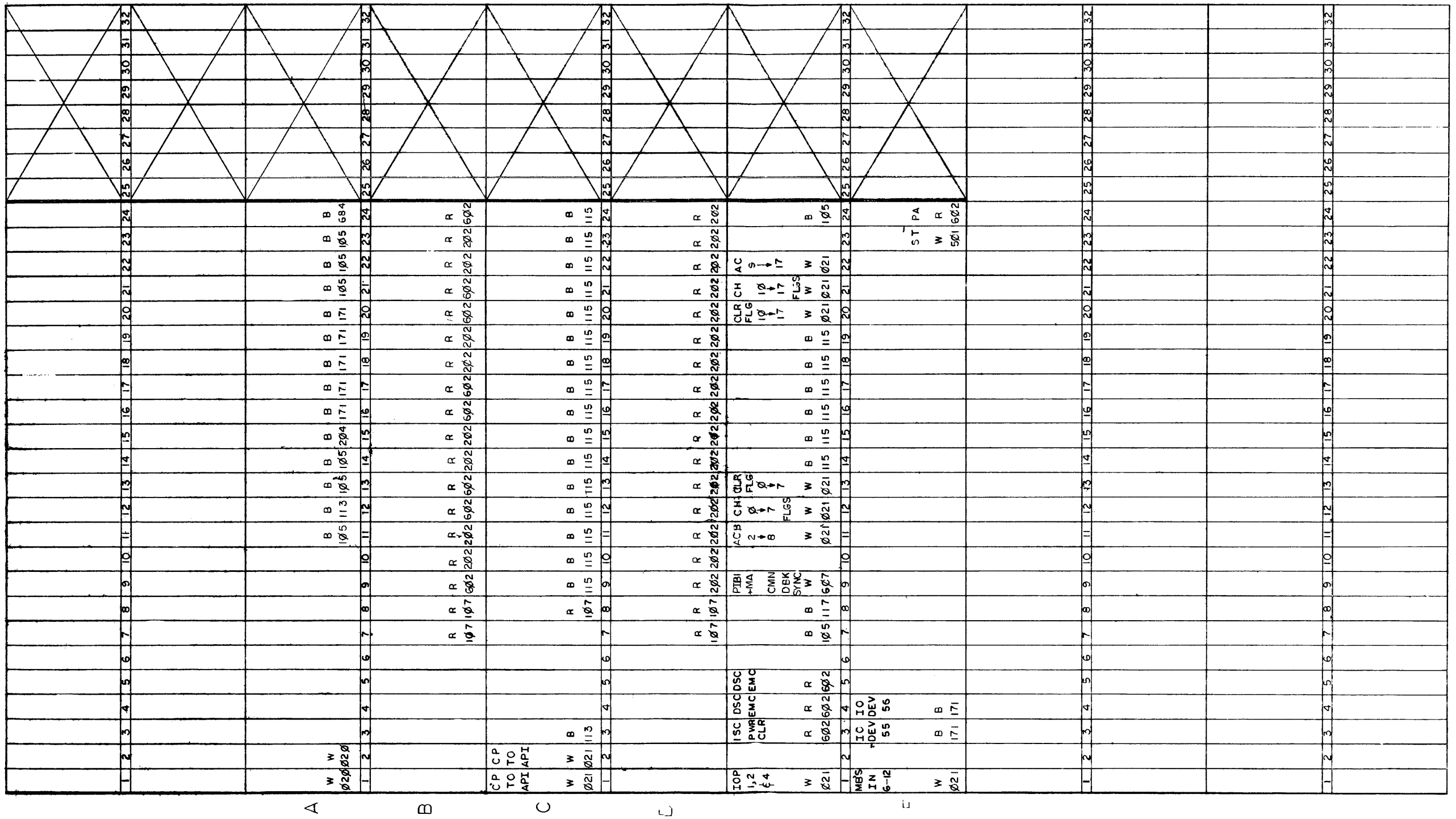
Automatic Priority Interrupt System (Sheet 1) BS-D-172-0-3



Automatic Priority Interrupt System (Sheet 2) BS-D-172-0-3

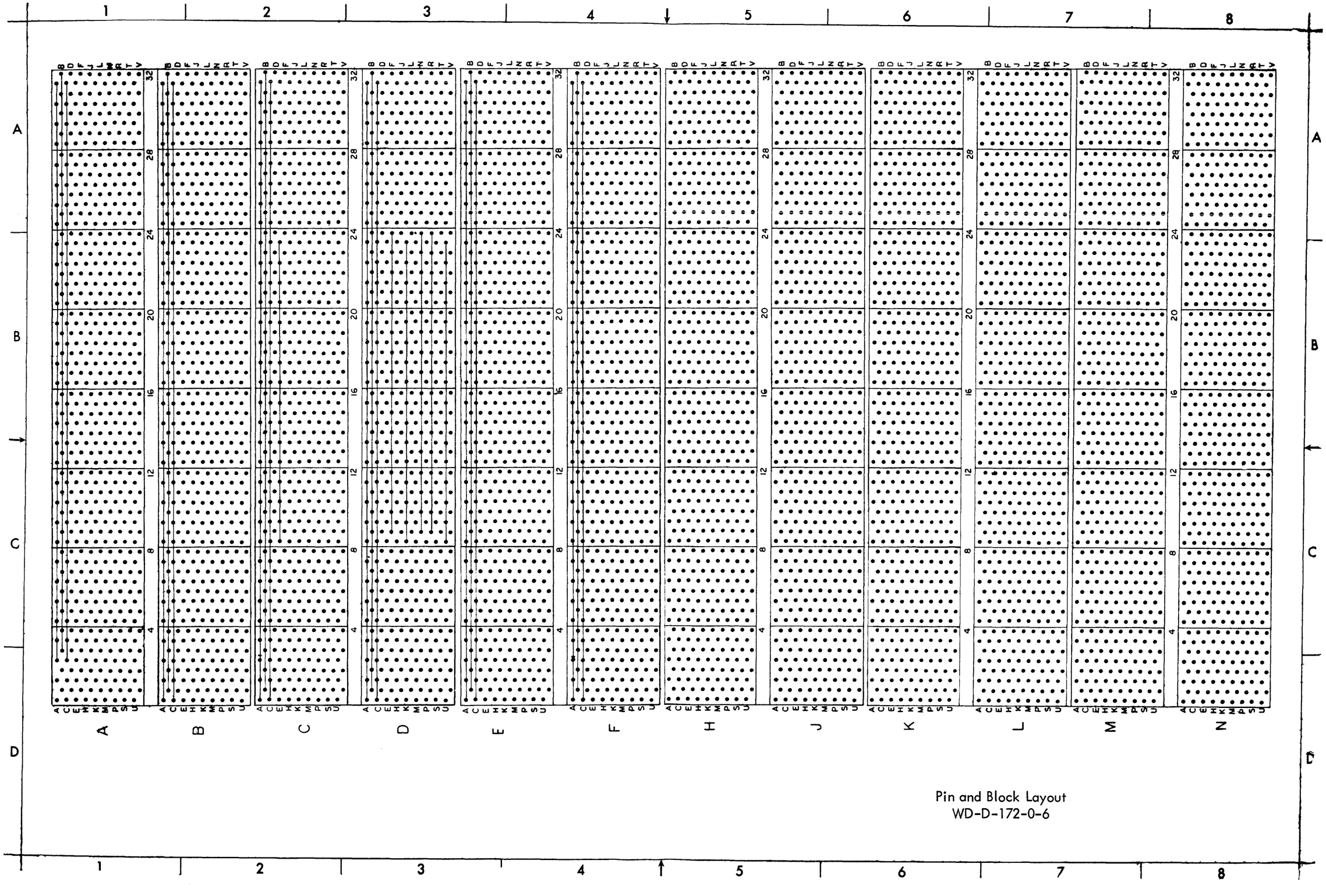
Automatic Priority Interrupt System (Sheet 2) BS-D-172-0-3

AUTOMATIC PRIORITY
INTERRUPT SYSTEM
BACK DOOR LOGIC



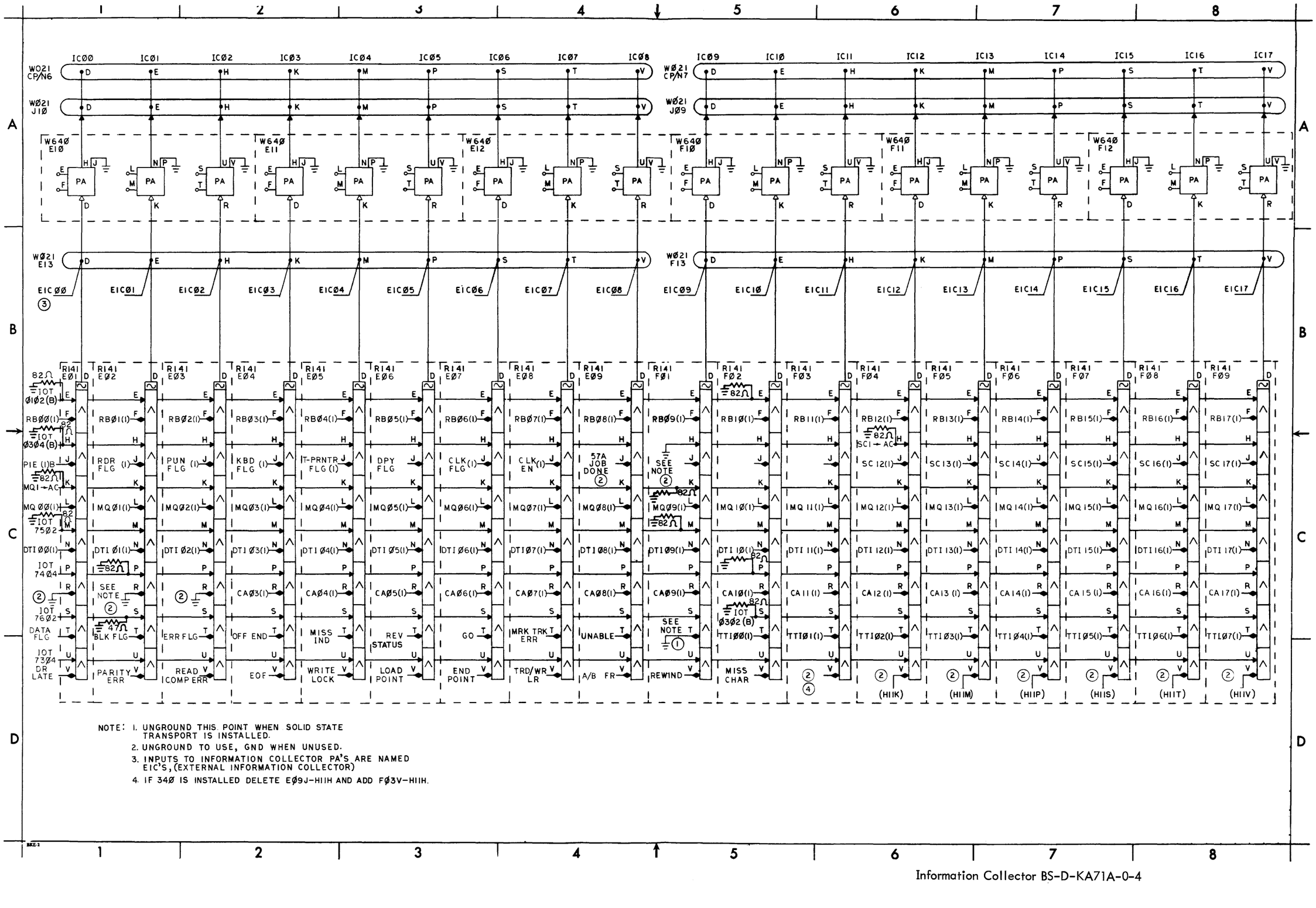
Module Map
ML-D-172-0-5

Module Map ML-D-172-0-5



Pin and Block Layout
WD-D-172-0-6

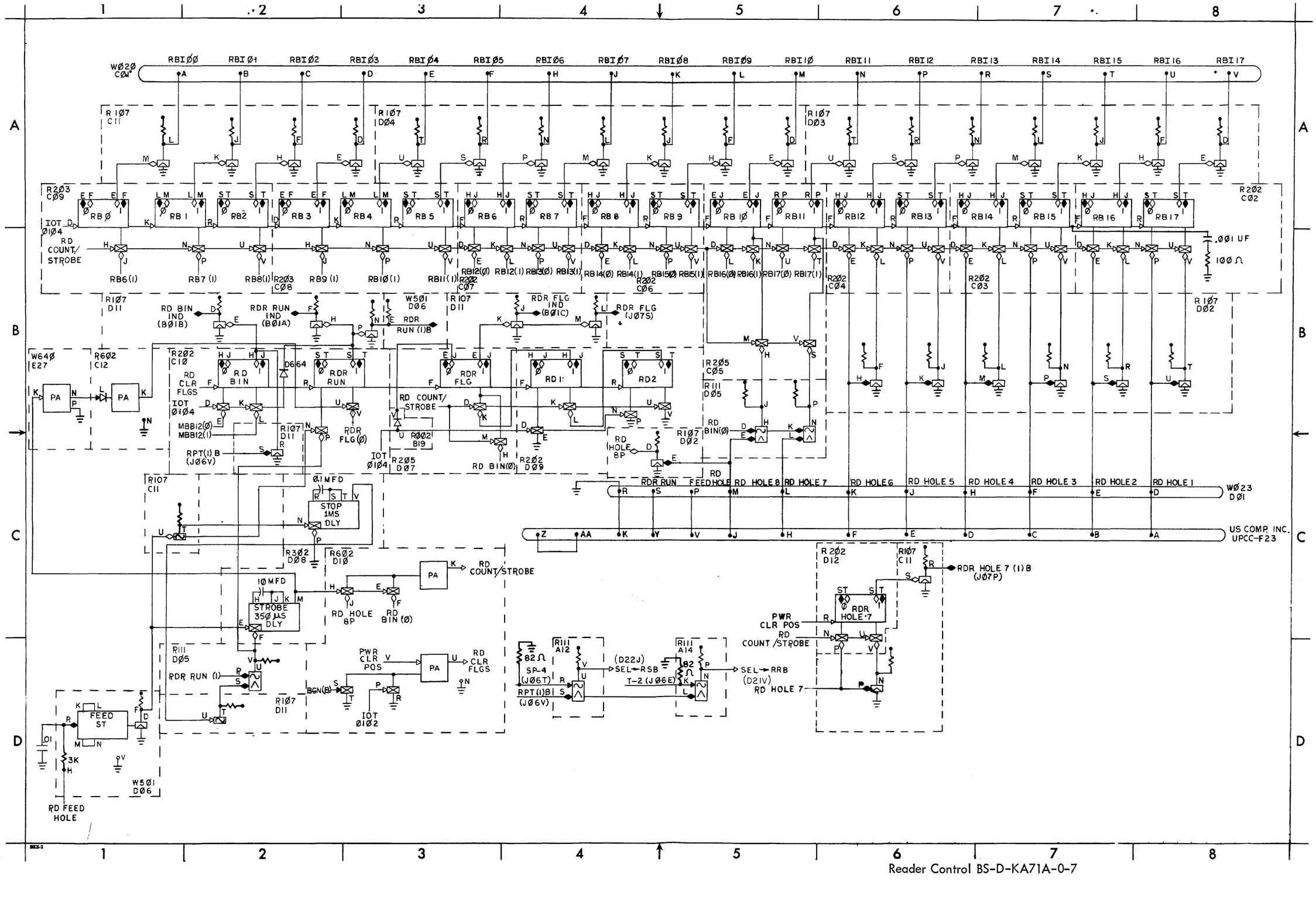
Pin and Block Layout WD-D-172-0-6



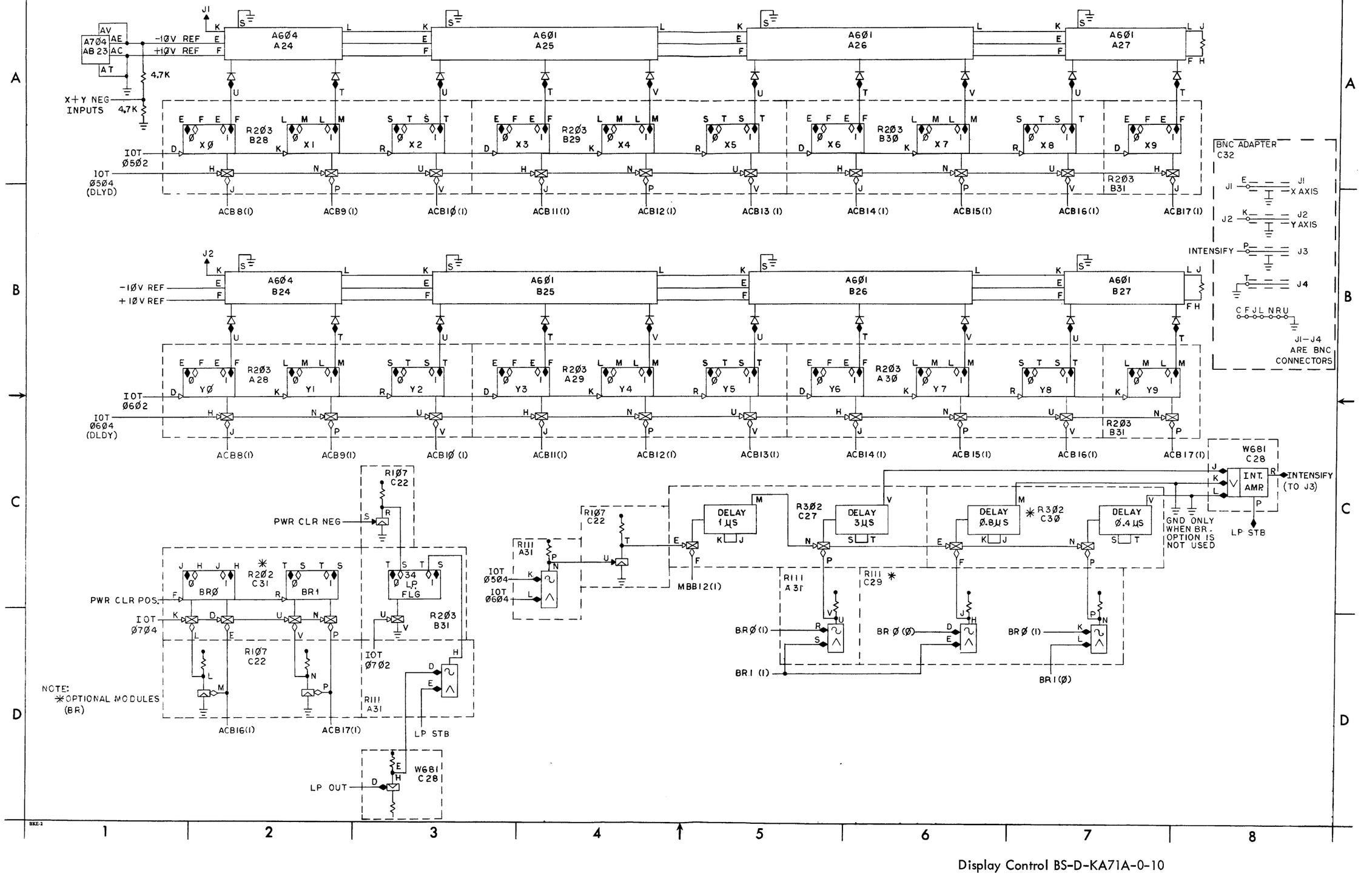
NOTE: 1. UNGROUND THIS POINT WHEN SOLID STATE TRANSPORT IS INSTALLED.
2. UNGROUND TO USE, GND WHEN UNUSED.
3. INPUTS TO INFORMATION COLLECTOR PA'S ARE NAMED EIC'S, (EXTERNAL INFORMATION COLLECTOR)
4. IF 34Ø IS INSTALLED DELETE EØ9J-HIIH AND ADD FØ3V-HIIH.

BKE-2

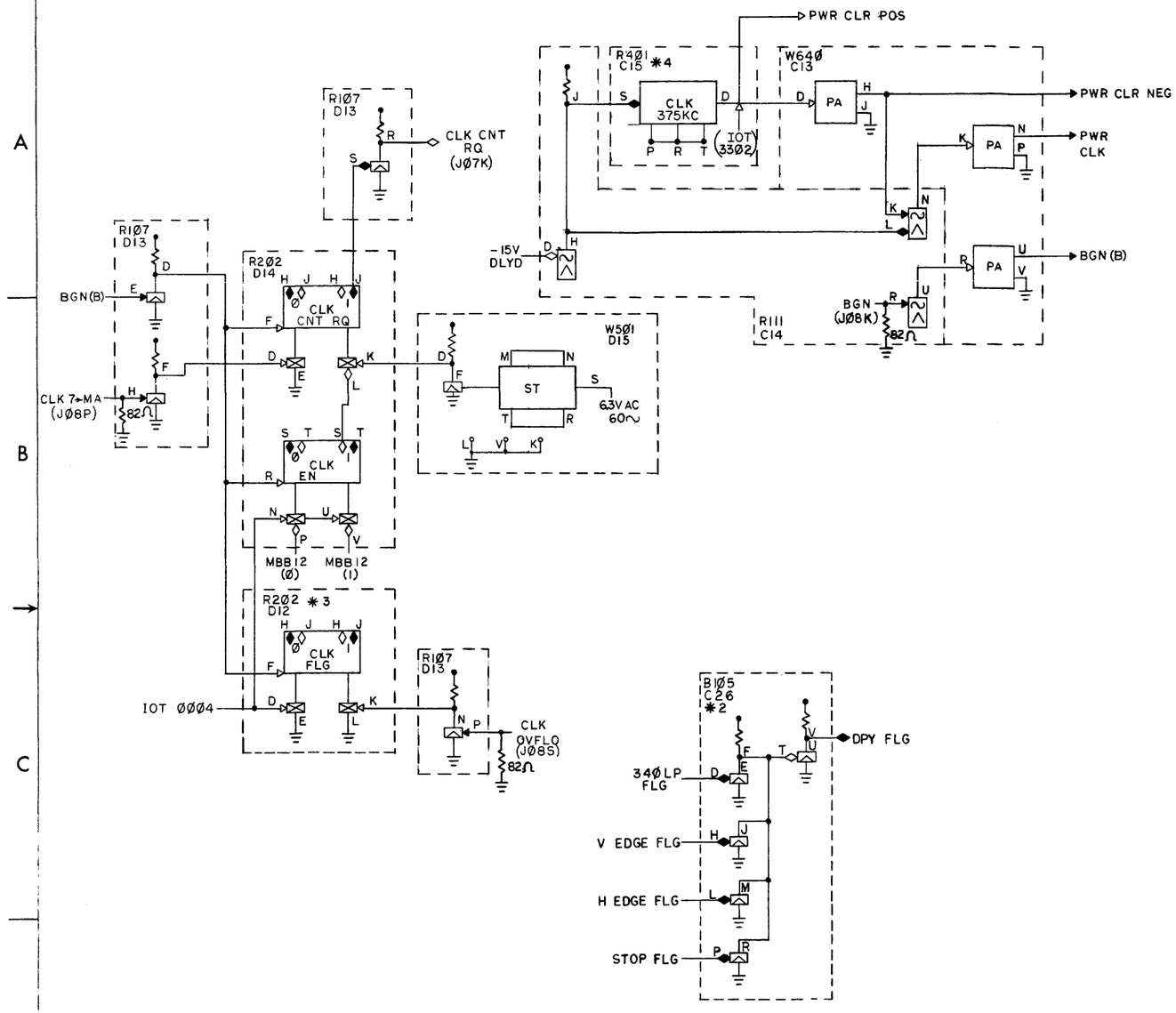
Information Collector BS-D-KA71A-0-4



Reader Control BS-D-KA71A-0-7



Display Control BS-D-KA71A-0-10



*1 THIS LOCATION CAN BE USED FOR CLOCK (TO REPLACE 60~)

*2 ADD A B105 IN C26 FOR 340 DISPLAY.

*3 2ND PART OF R 202 USED IN RDR CONTROL

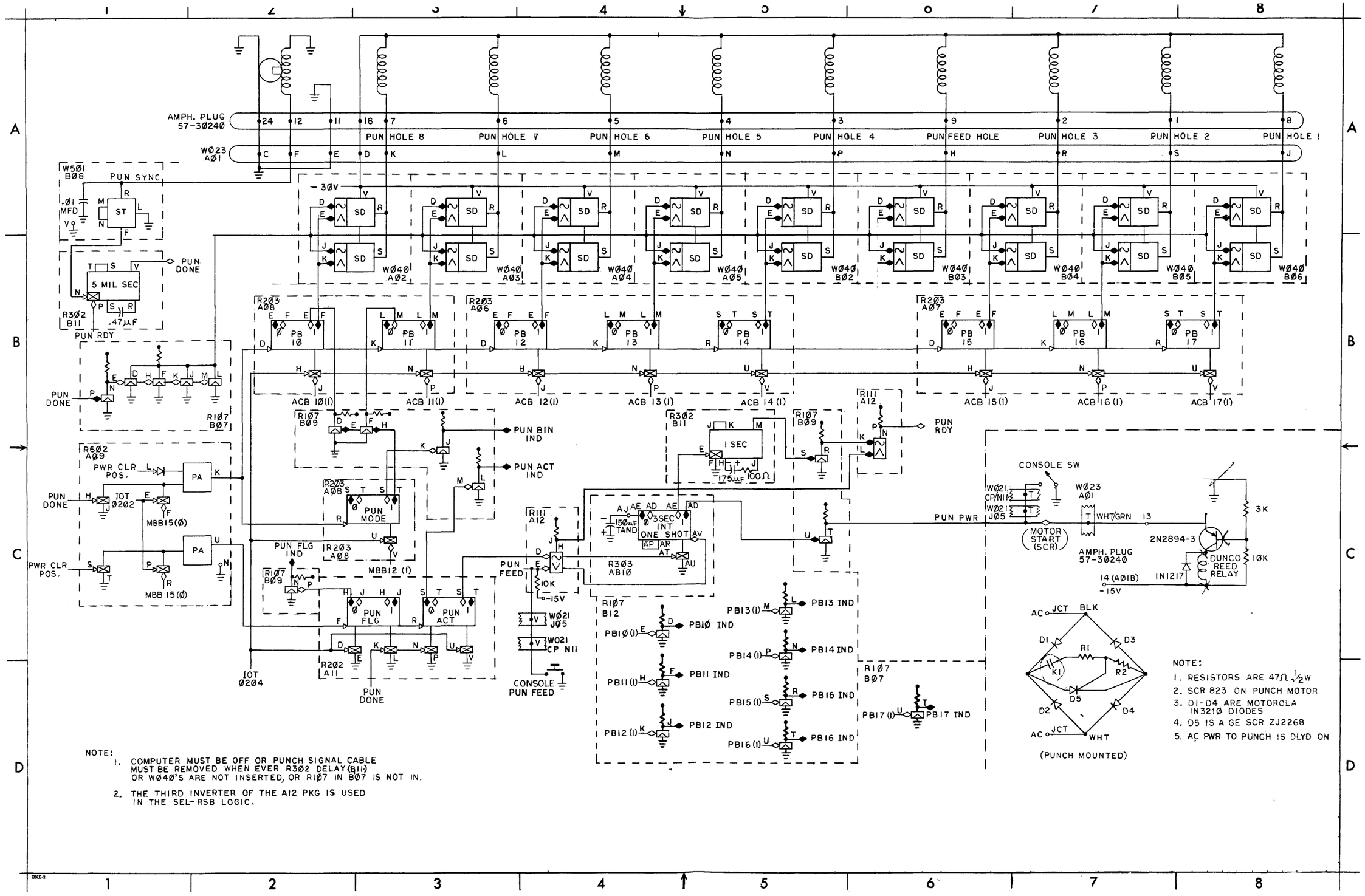
*4 NO ADJUSTMENT REQUIRED

*5 ADD FOR OPTION AS REQUIRED

BKE-2

CLK, FLG, SKP, and PWR CLR BS-D-KA71A-0-3

CLK, FLG, SKP, and PWR CLR BS-D-KA71A-0-3



NOTE:

1. COMPUTER MUST BE OFF OR PUNCH SIGNAL CABLE MUST BE REMOVED WHEN EVER R3Ø2 DELAY(B11) OR WØ4Ø'S ARE NOT INSERTED, OR RIØ7 IN BØ7 IS NOT IN.
2. THE THIRD INVERTER OF THE AI2 PKG IS USED IN THE SEL-RSB LOGIC.

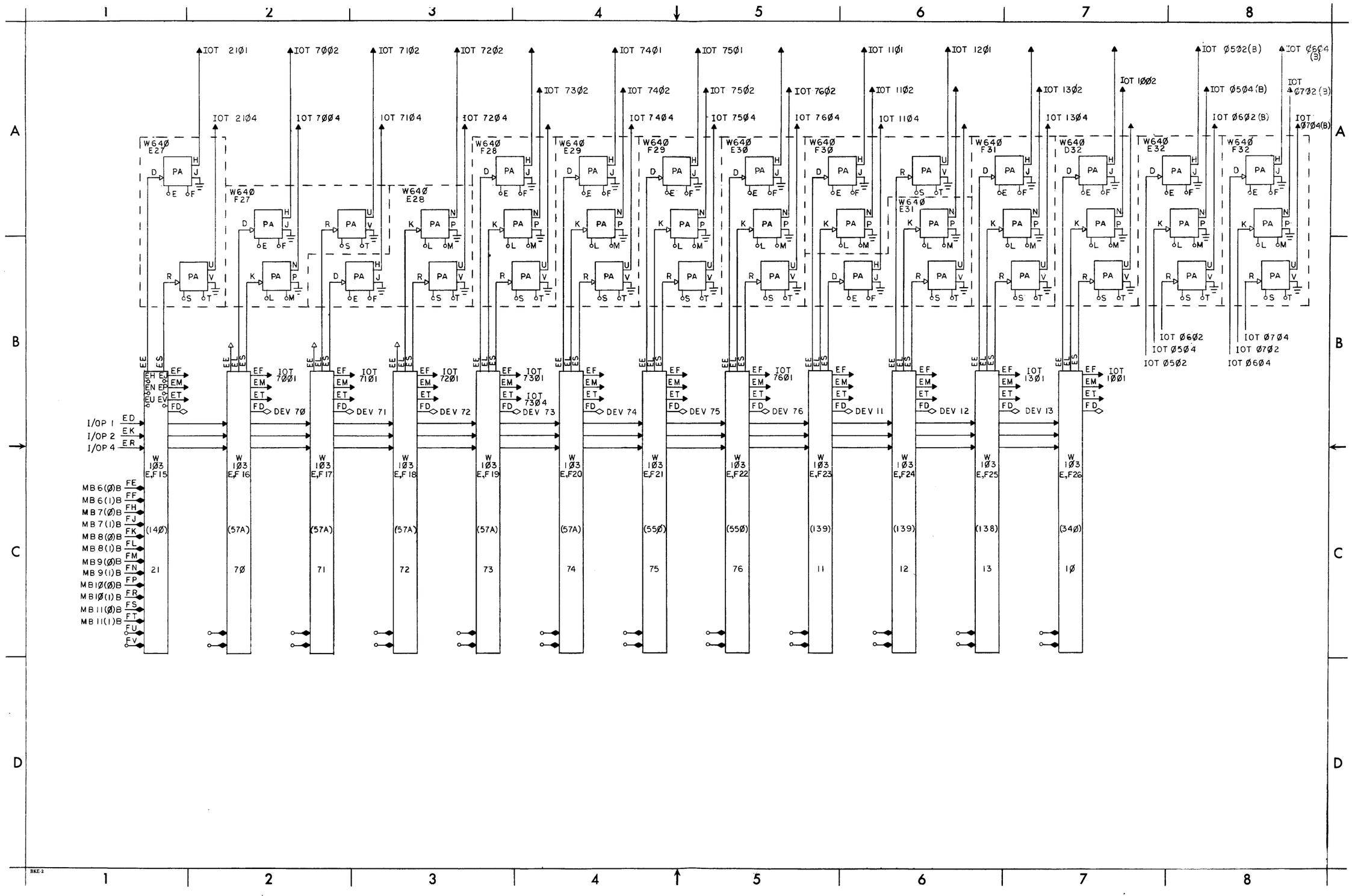
NOTE:

1. RESISTORS ARE 47Ω, ½W
2. SCR 823 ON PUNCH MOTOR
3. D1-D4 ARE MOTOROLA IN3210 DIODES
4. D5 IS A GE SCR ZJ2268
5. AC PWR TO PUNCH IS DLYD ON

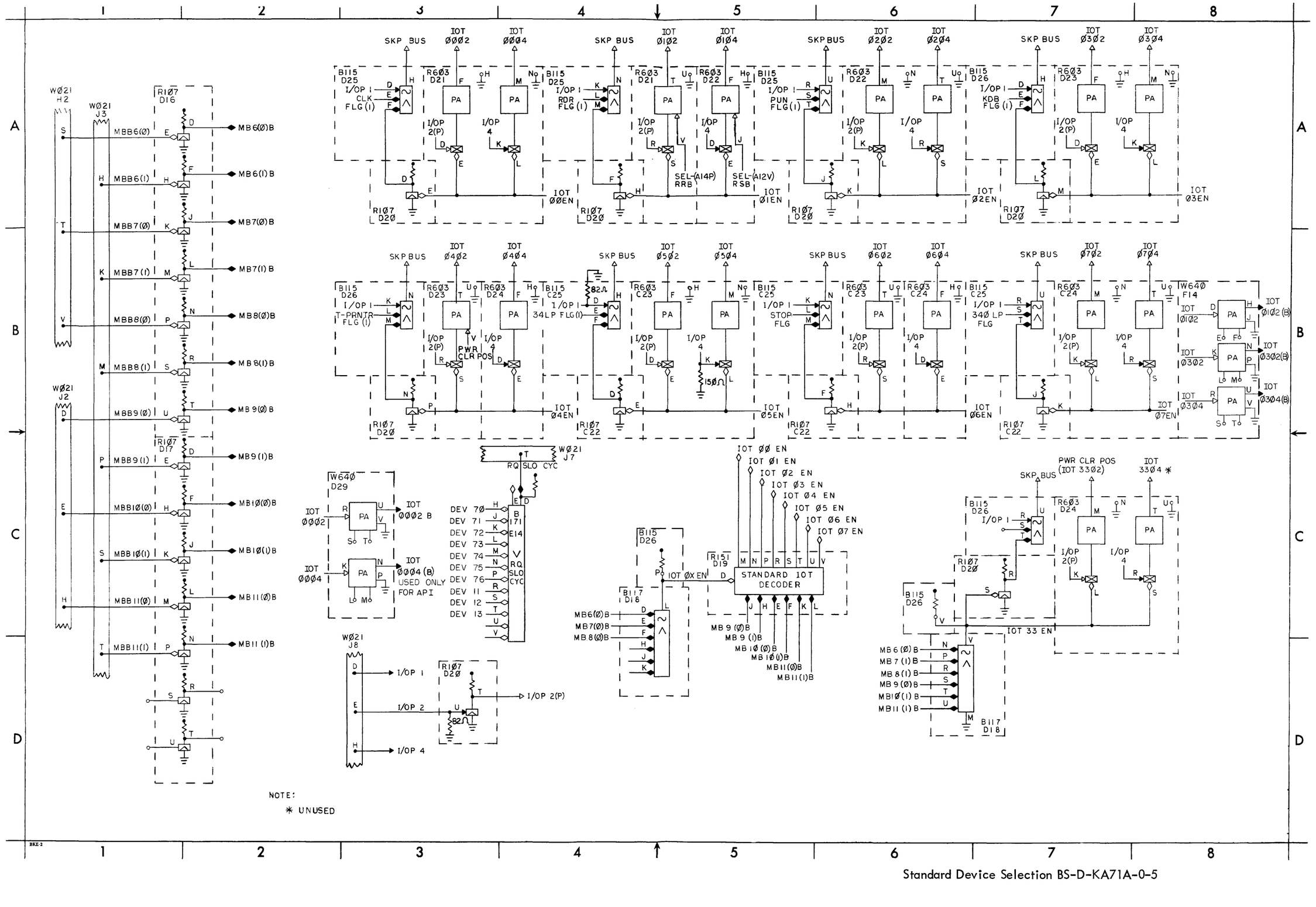
BKE-2

Punch Control BS-D-KA71A-0-8

Punch Control BS-D-KA71A-0-8



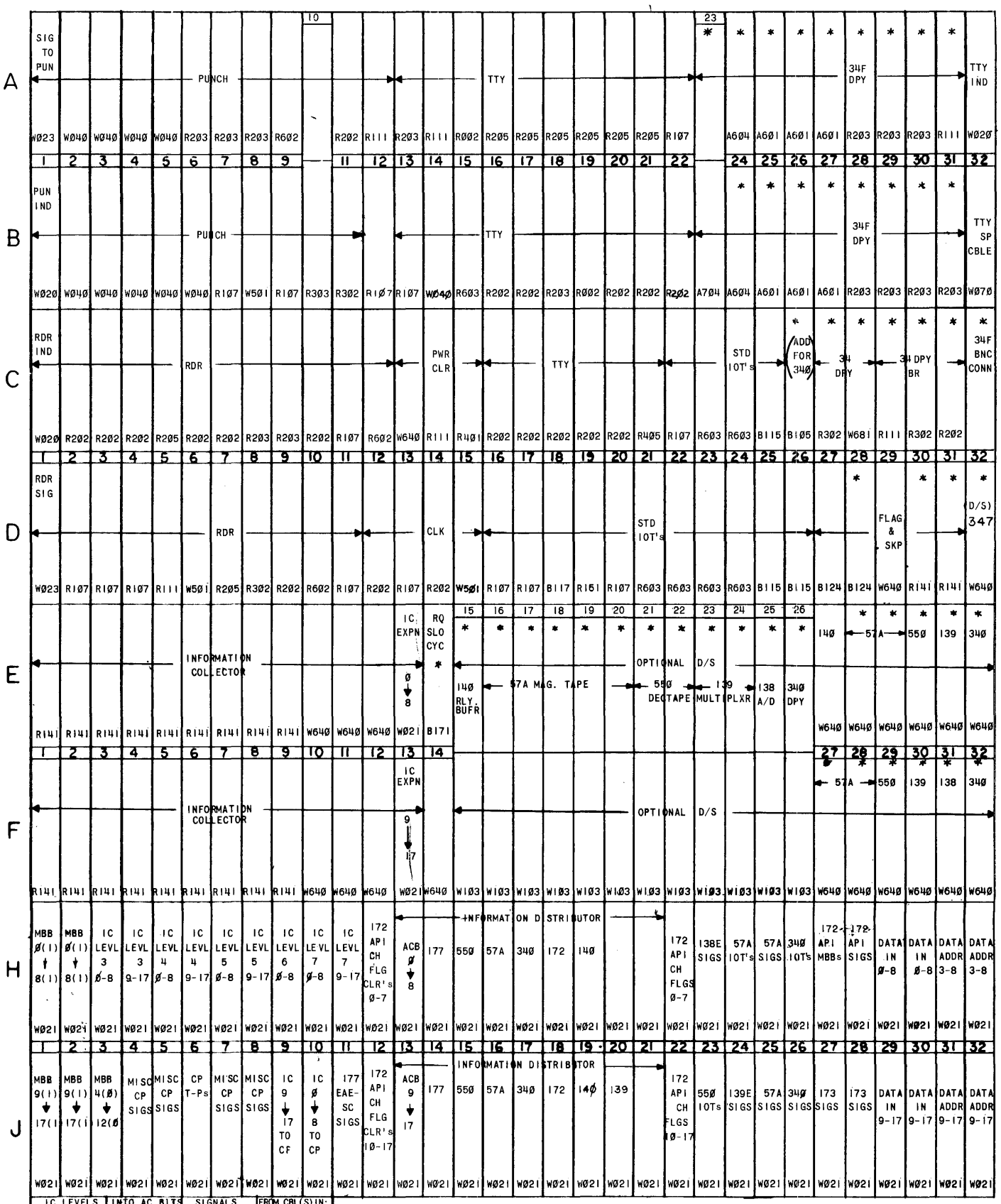
Optional Device Selection BS-D-KA71A-0-6


SKP BUS
IOT ØØØ2
IOT ØØØ4
IOT Ø1Ø2
IOT Ø1Ø4
IOT Ø2Ø2
IOT Ø2Ø4
IOT Ø3Ø2
IOT Ø3Ø4
IOT Ø4Ø2
IOT Ø4Ø4
IOT Ø5Ø2
IOT Ø5Ø4
IOT Ø6Ø2
IOT Ø6Ø4
IOT Ø7Ø2
IOT Ø7Ø4
B115 D25 I/OP 1 CLK FLG (1)
B115 D25 I/OP 1 RDR FLG (1)
B115 D25 I/OP 1 PUN FLG (1)
B115 D26 I/OP 1 KDB FLG (1)
B115 D26 I/OP 1 T-PRNTR FLG (1)
B115 C25 I/OP 1 34LP FLG (1)
B115 C25 I/OP 1 STOP FLG
B115 C25 I/OP 1 340 LP FLG
R6Ø3 D21
R6Ø3 D22
R6Ø3 D23
R6Ø3 D24
R6Ø3 C23
R6Ø3 C24
PA
I/OP 2(P)
I/OP 4
PWR CLR POS
SEL-(A14P) RRB
SEL-(A12V) RSB
82Ω
15ØΩ
RIØ7 D2Ø
RIØ7 C22
IOT ØØEN
IOT Ø1EN
IOT Ø2EN
IOT Ø3EN
IOT Ø4EN
IOT Ø5EN
IOT Ø6EN
IOT Ø7EN
W64Ø F14
IOT Ø1Ø2 (B)
IOT Ø3Ø2 (B)
IOT Ø3Ø4 (B)
WØ21 H2
WØ21 J3
WØ21 J2
RIØ7 D16
RIØ7 D17
MBB6(Ø)
MBB6(1)
MBB7(Ø)
MBB7(1)
MBB8(Ø)
MBB8(1)
MBB9(Ø)
MBB9(1)
MBBIØ(Ø)
MBBIØ(1)
MBB11(Ø)
MBB11(1)
MB6(Ø)B
MB6(1)B
MB7(Ø)B
MB7(1)B
MB8(Ø)B
MB8(1)B
MB9(Ø)B
MB9(1)B
MBIØ(Ø)B
MBIØ(1)B
MB11(Ø)B
MB11(1)B
W64Ø D29
IOT ØØØ2
IOT ØØØ2 B
IOT ØØØ4
IOT ØØØ4 (B) USED ONLY FOR API
WØ21 J7
RQ SLO CYC
B 17 E14
DEV 7Ø
DEV 71
DEV 72
DEV 73
DEV 74
DEV 75
DEV 76
DEV 11
DEV 12
DEV 13
WØ21 J8
I/OP 1
I/OP 2
I/OP 4
I/OP 2(P)
82Ω
B11 7 D18
IOT ØX EN
R15 D19
STANDARD IOT DECODER
IOT ØØ EN
IOT Ø1 EN
IOT Ø2 EN
IOT Ø3 EN
IOT Ø4 EN
IOT Ø5 EN
IOT Ø6 EN
IOT Ø7 EN
MB9(Ø)B
MB9(1)B
MBIØ(Ø)B
MBIØ(1)B
MB11(Ø)B
MB11(1)B
PWR CLR POS (IOT 3302)
IOT 3304 *
IOT 33 EN
MB6(Ø)B
MB7(1)B
MB8(1)B
MB9(Ø)B
MBIØ(1)B
MB11(1)B
B117 D18

NOTE:

* UNUSED

REVISIONS			
REV LTR	ECO NO	DATE	ENG
A	3	11-18 65	JS
B	6	12-2 65	RPB
C	7	12-17 65	RPB
D	11	1-17 66	RPB
E	13	1-27 66	RPB
F	15	2-7-66	RPB
H	21	5-20 66	RPB



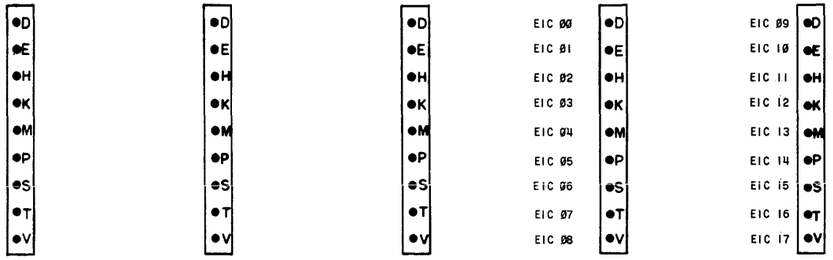
IC LEVELS	INTO AC BITS	SIGNALS	FROM CBL(S)IN:
1	Ø → 17	PAPER TAPE RDR RBØ → RB17	——
2	Ø → 8	I/O STATUS FLAGS	——
2	12 → 17	EAE SC12 → SC17	J11
3	Ø → 17	EAE MQØ → MQ17	HØ3 AND HØ4
4	Ø → 17	DECTAPE DTIØ → DTI17	HØ5 AND HØ6
5	3 → 17	57A: CA3 → CA17 340: CA5 → CA17 139: CA12 → CA17	57A: HØ7 & HØ8 340: HØ7 & HØ8 139: J24
6	Ø → 8	DECTAPE STATUS FLAGS	HØ9
6	10 → 17	TELETYPE TTI1 → TTI7	——
7	Ø → 8	57A: STATUS BITS 340: X REGISTER 138: ADRØ → ADR8	HIØ
7	9 → 17	57A: STATUS BITS 340: Y REGISTER 138: ADR9 → ADR11	H11

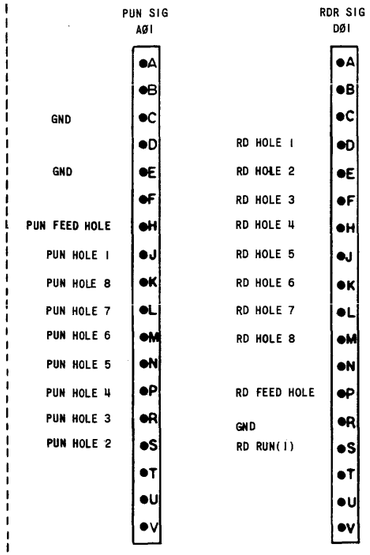
* NOT INCLUDED IN STANDARD COMPUTER

STANDARD MODULES		OPTIONAL MODULES		
TYPE	QUANTITY	OPTION	TYPE	QUANTITY
B115	3	34F DISPLAY	A6Ø1	6
B117	1		A6Ø4	2
B124	1		A7Ø4	1
RØØ2	2		R111	2
R107	14		R202	1
R111	4		R203	7
R141	19		R302	2
R151	1		W681	1
R202	19	340 DISPLAY	B105	1
R203	7	FLG & SKP	B124	1
R205	8		R141	2
R302	2		W640	1
R303	1	RQ SLO CYCLE	B171	1
R401	1	OPTIONAL D/S	W103	12
R405	1		W640	11
R602	3			
R603	7			
WØ4Ø	10			
W501	3			
W640	10			

Module Location for I/O ML-D-KA71A-0-2

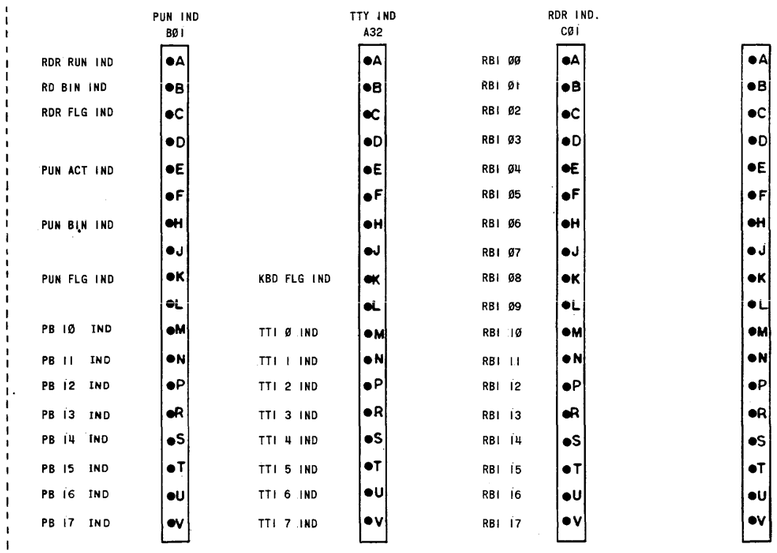
WØ21 SIGNAL CABLE CONNECTORS

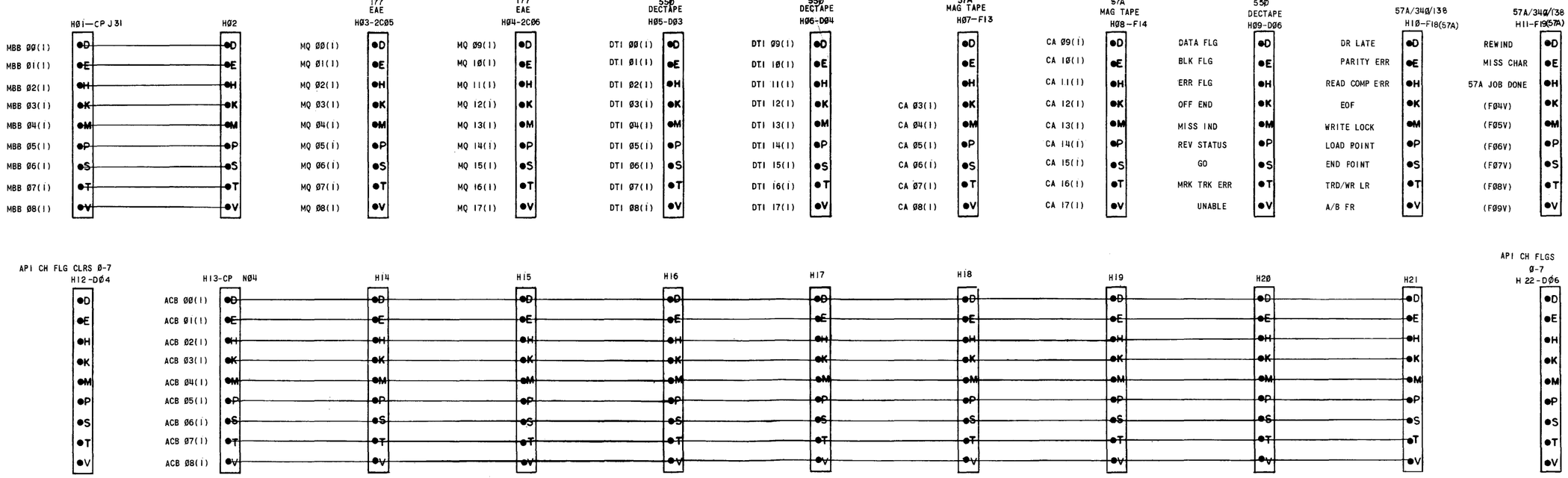




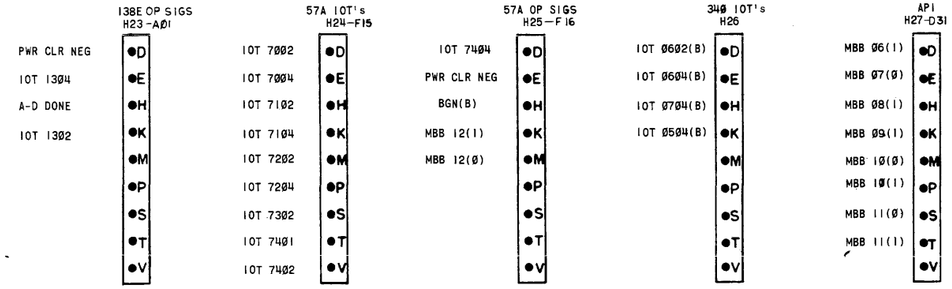
WØ23 SIGNAL CABLE CONNECTORS

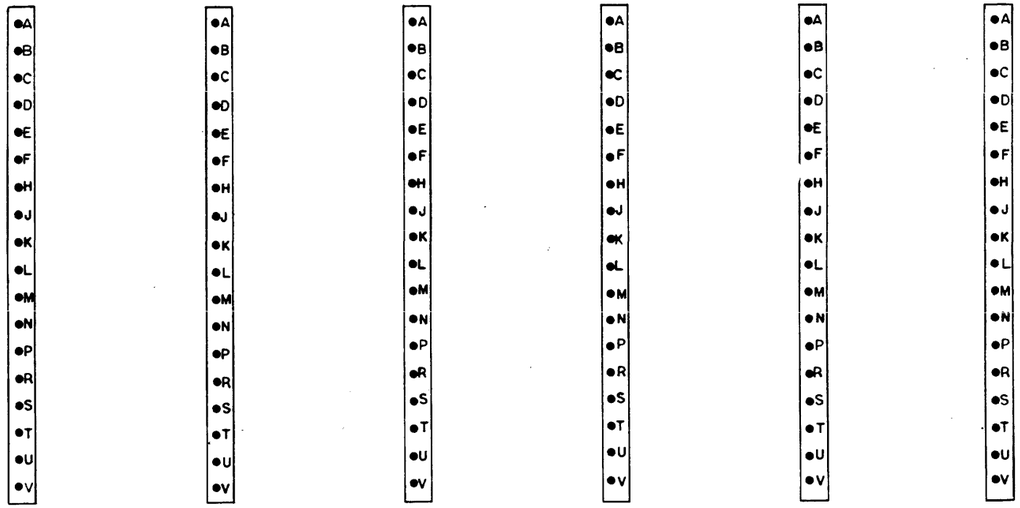
WØ2Ø INDICATOR CABLE CONNECTORS

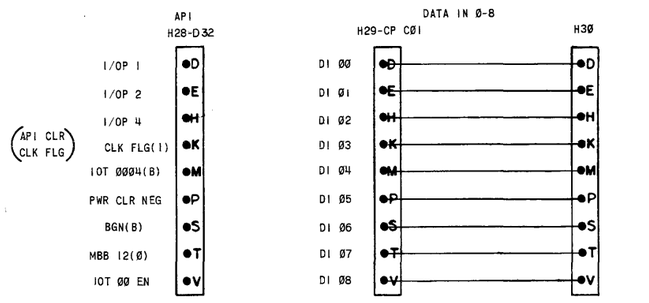


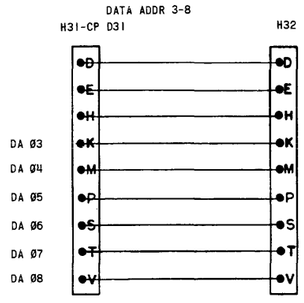


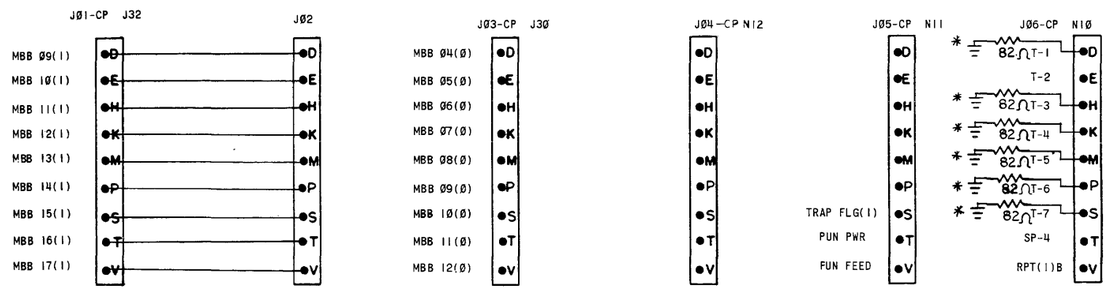
I/O Package Cables (Sheet 1) CD-D-KA71A-0-11

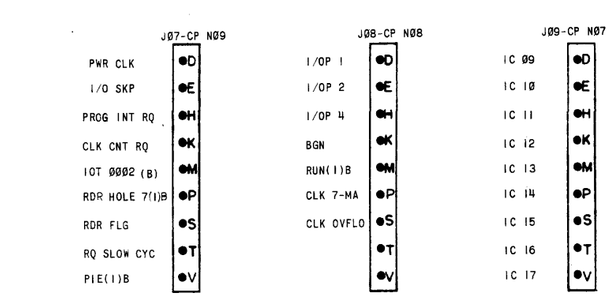


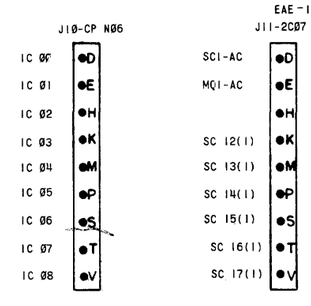


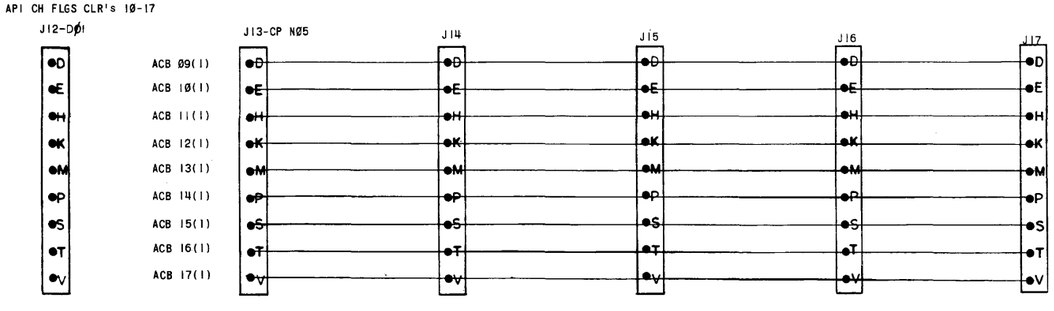








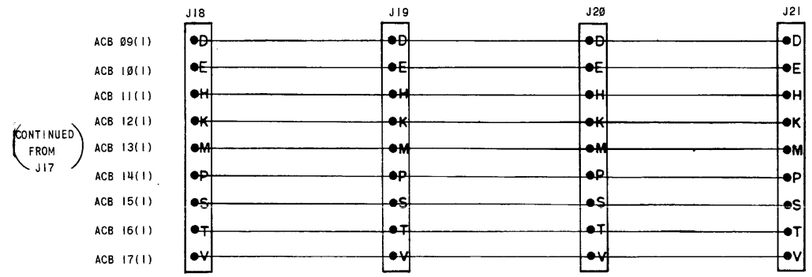


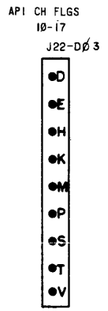


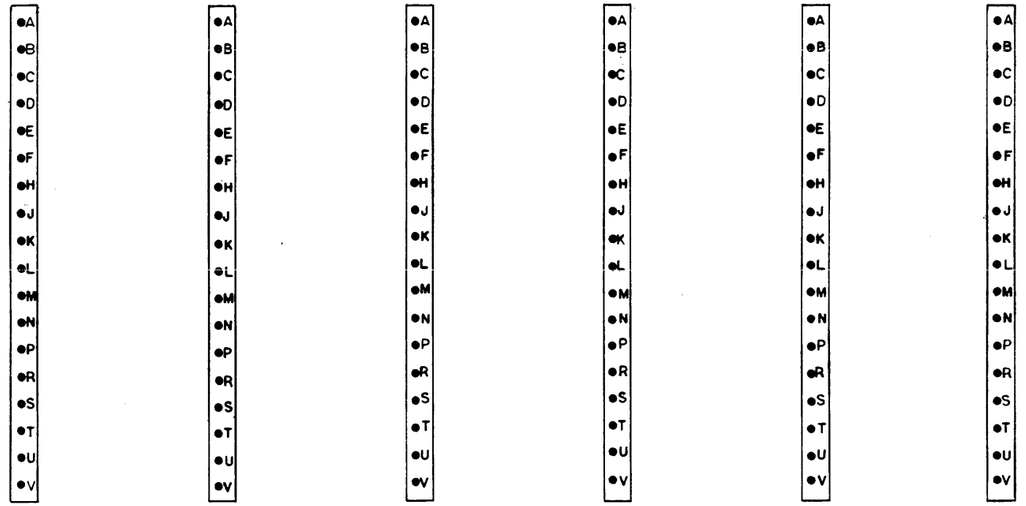
* THIS TERMINATION IS ADDED BECAUSE T1,T3-T7 ARE NOT USED EXCEPT WITH CERTAIN PERIPHERAL DEVICE-WHEN USED IN SOME DEVICE, THIS TERMINATION SHOULD BE MOVED TO THE END OF THE PULSE LINE.

I/O Package Cables (Sheet 2) CD-D-KA71A-0-11

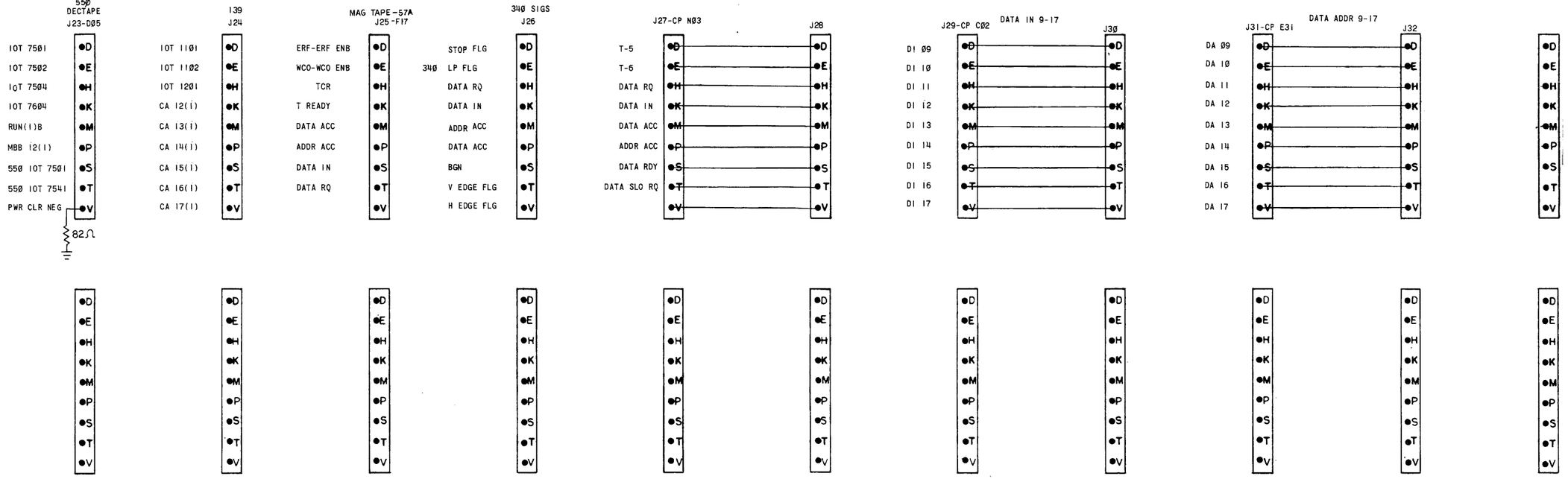
WØ21 SIGNAL CABLE CONNECTORS







WØ2Ø INDICATOR CABLE CONNECTORS



I/O Package Cables (Sheet 3) CD-D-KA71A-0-11

A
B
C
D
E
F
H
J
K
L
M
N
A C E H K M P S U
4
8
12
16
20
24
28
32
B D F J L N R T V

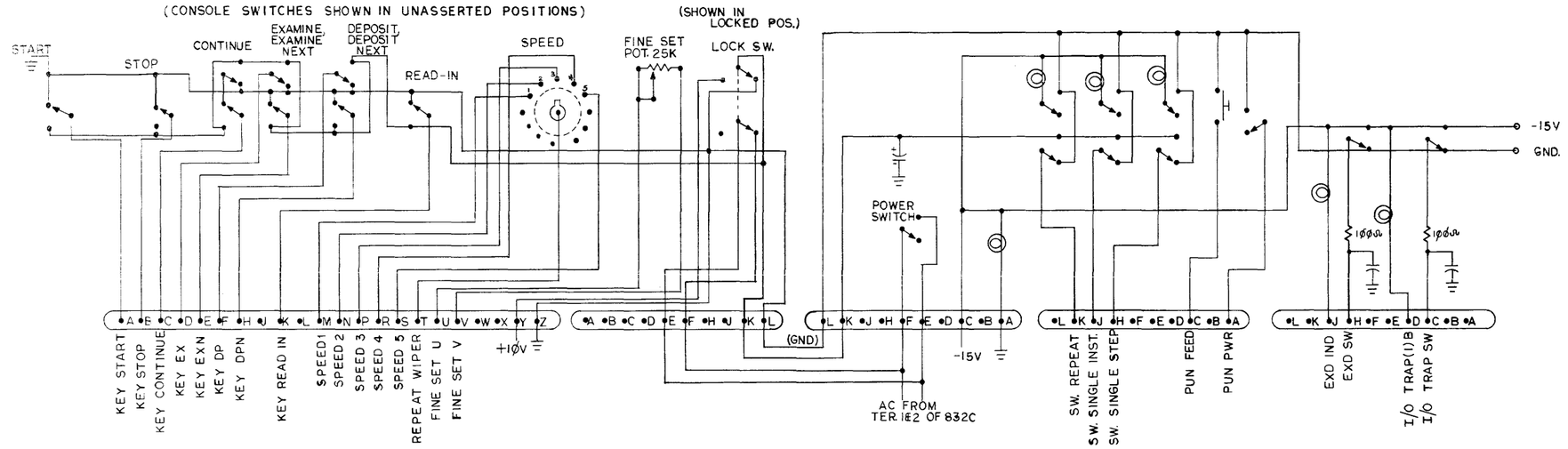
I/O Package Bus Schedule WD-D-KA71A-0-12

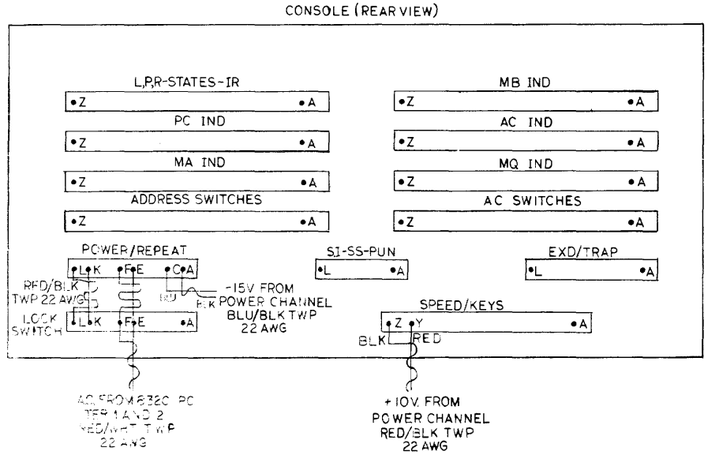
TERMINATOR VALUE	POL	PIN	PIN	RUN NAME
150ufd CAP. @ 15VDC		A1ØJ(-)	GND(+)	
1ØK OHM RES.		A12E	-15V	PUN FEED
82 OHM RES.		A12R	GND	SP-4
82 OHM RES.		A14K	GND	T-2
.01ufd DISC CAPACITOR		BØ8R	GND	PUN SYNC
175ufd/15 VDC AND 1ØØ OHM IN SERIES		B11H(-)	B11J(+)	
.47ufd CAP.		B11R	B11S	
.ØØ1ufd DISC & 1ØØ OHM IN SERIES		CØ2F	GND	IOT Ø1Ø4
82 OHM RES.		C14R	GND	BGN
.ØØ1ufd DISC & 1ØØ OHM IN SERIES		C17R	GND	TTI CLR CNT
15Ø OHM RES.		C23K	GND	I/OP-4
82 OHM RES.		C25D	GND	I/OP-1
.01 ufd disc Cap		DO6R	GND	
3K 1/4 W 5%		D06H	D06R	RDR FEED HOLE
Ø.1ufd DISC @ 50 VDC		DØ8H	DØ8J	
.Ø.1ufd DISC CAPACITOR		DØ8R	DØ8T	
82 OHM RES		D13H	GND	CLK 7 → MA
D664 DIODE		C1ØK	C1ØS	K ●——▶●S
82 OHM RES.		D13P	GND	CLK OVFLO
82 OHM RES.		D2ØU	GND	I/OP-2
82 OHM RES.		D3ØU	GND	55Ø IOT 75Ø1
82 OHM RES.		D31E	GND	55Ø IOT 7541

Terminator List (Sheet 1) TL-A-KA71A-0-14

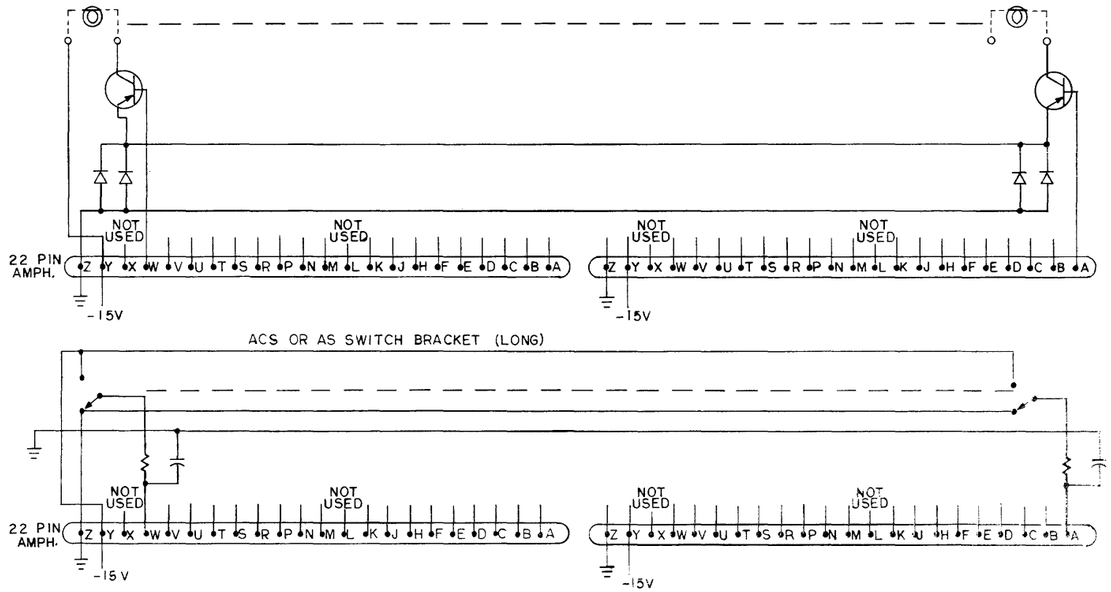
TERMINATOR VALUE	POL	PIN	PIN	RUN NAME
82 OHM RESISTOR		EØ1E	GND	IOT Ø1Ø2(B)
" " "		EØ1H	"	IOT Ø3Ø4(B)
" " "		EØ1K	"	MQ 1 ⟶ AC
" " "		EØ1M	"	IOT 75Ø2
" " "		EØ2P	"	IOT 74Ø4
47 OHM RESISTOR		EØ2S	"	IOT 76Ø2
82 OHM RESISTOR		FØ1K	"	MQ1 ⟶ AC
" " "		FØ1M	"	IOT 75Ø2
" " "		FØ2E	"	IOT Ø1Ø2(B)
" " "		FØ2P	"	IOT 74Ø4
" " "		FØ2S	"	IOT Ø3Ø2(B)
" " "		FØ4H	"	SC1 ⟶ AC
82 OHM RESISTOR		JØ6D	GND	T-1
" " "		JØ6H	"	T-3
" " "		JØ6K	"	T-4
" " "		JØ6M	"	T-5
" " "		JØ6P	"	T-6
" " "		JØ6S	"	T-7
" " "		J23V	"C23	PWR CLR NEG

Terminator List (Sheet 2) TL-A-KA71A-0-14



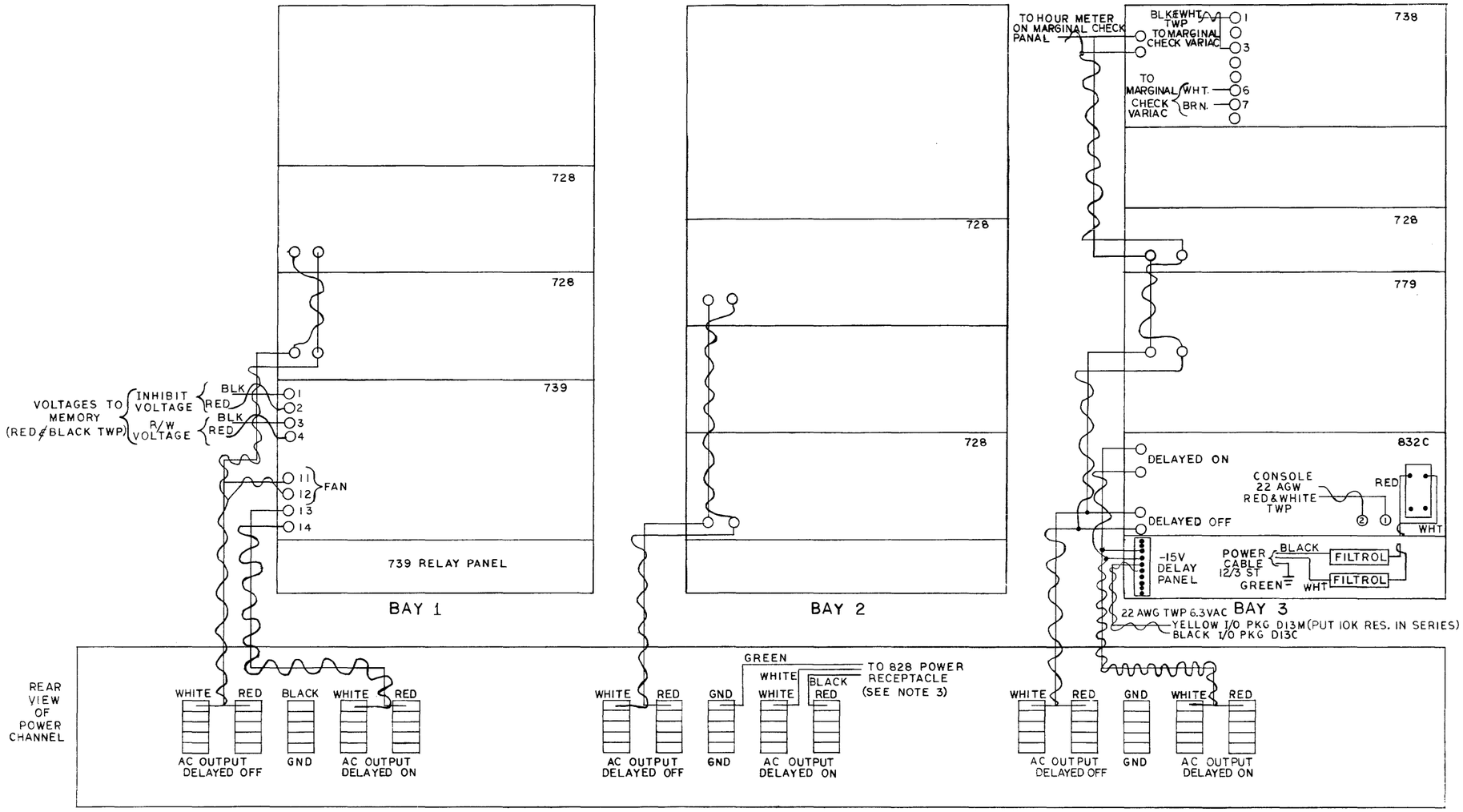


NOTE: UNLESS OTHERWISE INDICATED;
1 ALL RESISTORS ARE 10K 1/4 W
2 ALL CAPACITORS ARE 3.9 MFD 10V



Console Panel Wiring Diagram WD-D-7A-0-2

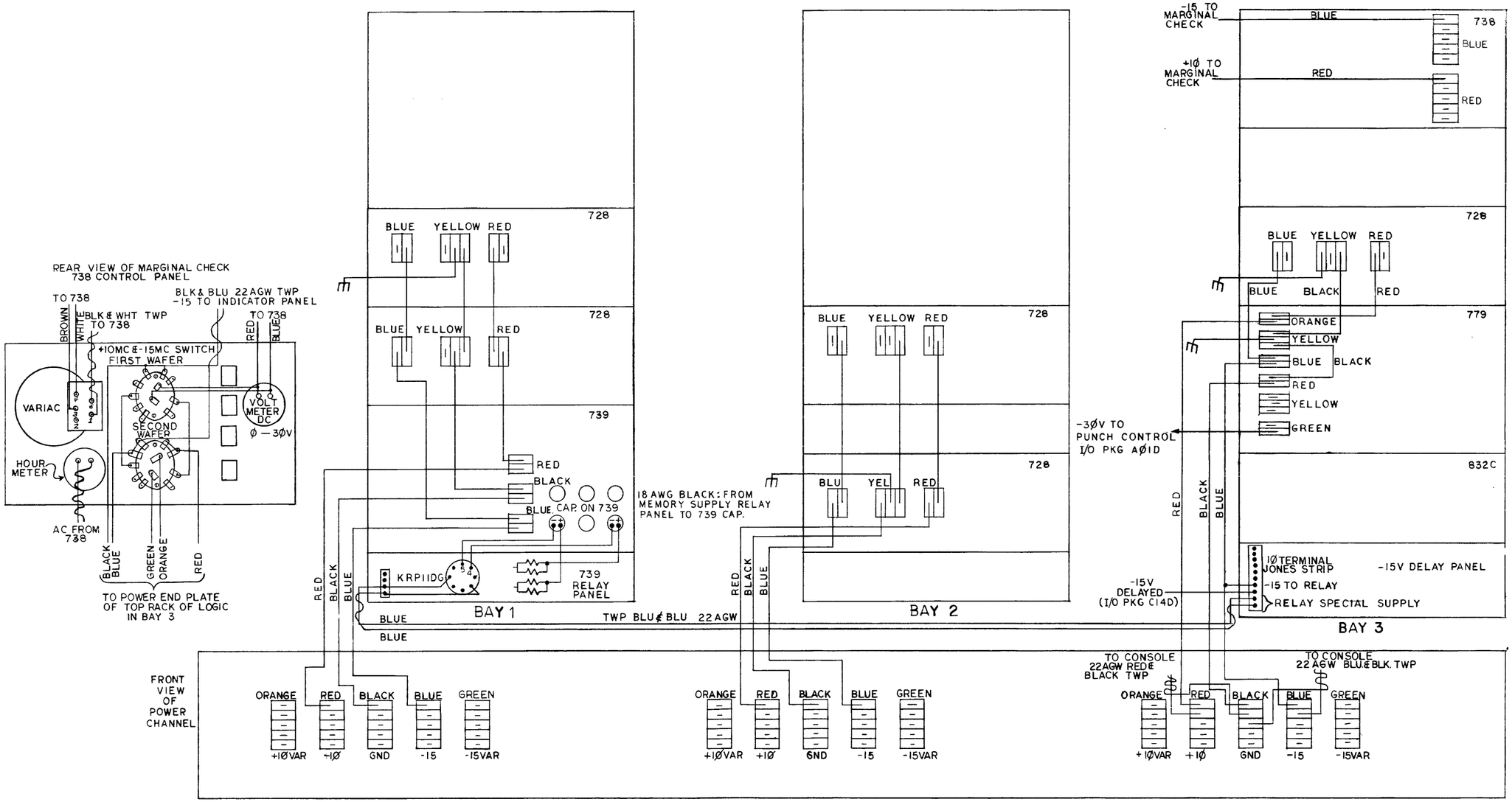
Console Panel Wiring Diagram WD-D-7A-0-2



NOTE:

1. ALL AC POWER WIRING TO BE IN 14 GAGE RED&WHITE TWP EXCEPT WHERE NOTED
2. FANS TO BE WIRED TO DELAYED OFF OUTPUT IN CHANNEL
3. MALE PLUG IN REAR OF 828 POWER RECEPTACLE SHOULD BE WIRED TO DELAYED ON IN POWER CHANNEL (BAY 2). THE READER, PUNCH, TELETYPE, AND OSCILLOSCOPE (34 DISPLAY, OPTIONAL) SHOULD BE WIRED TO THE FOUR FEMALE SOCKETS IN REAR OF 828.

AC Power Wiring PW-D-7A-0-3



NOTE:

1. ALL WIRING TO BE 14 AGW EXCEPT WHERE NOTED
2. POWER WIRING TO BOTTOM POWER END PLATE IN EACH BAY TO COME FROM POWER CHANNEL IN THAT BAY

DC Power Wiring PW-D-7A-0-4